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First and Second Order Digital Circuits with Neuronal Models under Pulses Train Stimulus

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Abstract. One or more neurons can be perceived as an analog circuit in terms of their voltage-time characteristics, but at the block level, they can rather fulfill a logic function. This later approach is imposed by the neuron membrane behavior that always works between two voltage levels – the resting potential and the acting potential, easily associated to two binary states. These levels change when an appropriate combination of pulses trains appears on the neuron's exciting and inhibiting input synapses. Being difficult to describe in all details the neuronal processes inside the human brain, this paper proposes some digital models able to mimic these biological processes. The first original element of this paper is the extension of the neuronal models, previously presented, from 0-order logic circuits to 1-order logic and 2-order logic circuits. The envelope signal shelters the pulses train that stimulate any neuron, and this envelope signal signature as the digital function represents an element of originality.

Key-words: Circuits; flip-flop; logic block; neurons; pulses train.

1. Introduction

In recent years, the neuromorphic computing community developed a serious interest to mimic neurons behavior by electronic circuits, using the fundamental research achievements and neuronal networks theory as in [1] and [2]. The traditional perceptron model is still actual, even

if it is a simplified one, being based on the instantaneous summation of dendritic input signals as in discussed [3] and [4]. This paper brings into discussion the logic circuits implementation by neuronal electronic block models, being a continuation of some recent published papers like [5]. Taking into account the neuron's behavior as a pulsed circuit that works with pulse trains of certain frequencies, the logic functions are fulfilled on the pulses envelope, not on the pulses themselves. At the logic level, this model treats the presence of a pulses train having a certain frequency as the logic value of 1, and the absence of a pulses train as the logic value of 0. In real life, the number of steps on the effort intensities scale is grown on behalf of both the number of the α-motoneurons simultaneously recruited and their size. The number of synapses is important for the α-motoneurons recruiting and increases through training. Based on the type of the effort, the synapses of descending neuronal columns can increase with α-motoneurons of a particular size (small, medium or large size). Independent of their size, the α-motoneurons that are driving the same muscle are working like systems being organized in neuronal pools [3]. Secondary γ-motoneurons and Renshaw interneurons complete the neuronal pools systems, making them systems with feedback [6]. At the cortex level, the neural networks are also reshaped by creating new memory circuits using new axonal dendritic feedback connections between neurons. Neuroscience frequently associates the neuron with an analog circuit as in [4], but its digital approach is almost missing [2]. Based on our previous neuron model depicted at transistor level [5], we replicated in simulations the logic NOT, AND and NOR functions that the neurons are able to obey for the combination of the pulses trains envelopes. It is an established fact that any logic function can be written as a composition of a few basic logic functions like NOT, AND, and NOR, which are exactly the basic functions modeled developed in a previous paper [5]. The general schematic for the "Neuron" block used for the neuronal gates is given in Fig. 1. According to their role in the nervous system, neurons can have different characteristics. Dotted lines in Fig. 1 underscore this fact. The components on the schematic bounded by dotted or dash-dotted lines are used or not, based on the modeled chosen role.

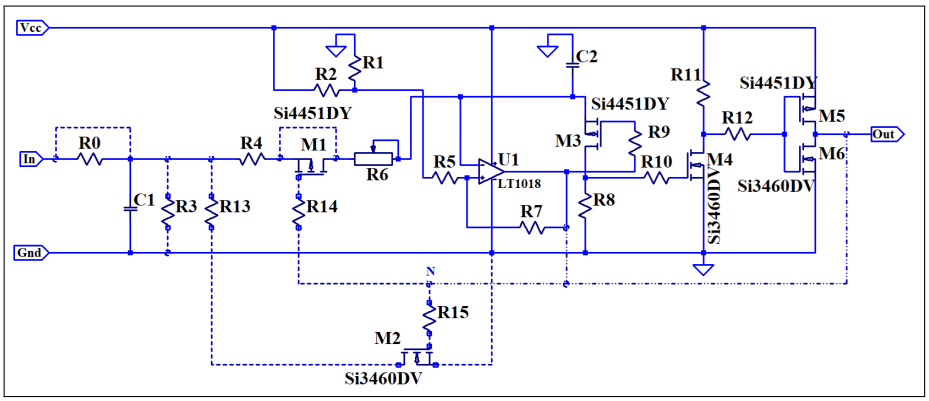

Fig. 1. Generic neuron block circuit schematic.

The voltage divider R1, R2 contribute with R5, R7 to establish the necessary thresholds for "U1" output to switch from supply voltage level of 5V to 0V and for the opposite transition, this commutation being the key for pulses generation on output. The pulses frequency can mainly be set by the resistor R4 and potentiometer R6. C1, mainly, simulates the membrane capacity and R3, R4, R6 simulates the membrane resistance. The values of C2, R8 fix the pulses duty

time. M1 and M2 are used, not necessarily together, for the in/out linearization of the neuronal block on the entire [0 .. 100] pulses/sec domain, otherwise supplementary output pulses or pulses bursts could appear. In these simulations, only M1 is used, see Table 1.

2. Neuronal 1-st and 2-nd order logic circuits

The goal of this paper is the simulation of the flip-flop circuits using neurons. In [7], these circuits are described as a promising topology.

2.1. The neuronal RS latch

The RS latch neuronal test circuit implementation is given in Fig. 2. To accomplish the excitation signals, some voltage signal supplies and logical AND circuits from LTSpice XVII simulation environment are used. The input signal "R" is achieved by the voltage signal supplies V2 and V2c, while the input signal "S" is achieved by the voltage signal supplies V3 and V3c. V2 and V3 are the carrier signal supply while V2c and V3c are the envelope signal supplies. The signal description for V2, V2c, V3, V3c is given at the bottom, Fig. 2. The pulsed carrier signal sources are out of phase, with a delay of 0.01s, to point out the behavior of the gate blocks like neuronal logic functions, based on neuronal integrative blocks. The neuronal RS latch schematic part, delimited by a dash-dot rectangle, preserves the original topology of the RS latch, being implemented with neuronal NOR circuits. As it can be seen from the signal diagram given in Fig. 3 when a train of pulses arises on "S" while "R" is "0" the output Q of the neuronal RS will be set to "1", and remains "1" even if "S" becomes "0" again, until a train of pulses appears on "R" resetting Q to "0" and setting Q- to "1", and so on. In Fig. 3 V(r), V(s), V(q) and V(q-) are the voltages at the R, S, Q and Q- terminals of the RS latch.

2.2. The neuronal JK latch

The JK latch is an improvement of the RS latch, dealing with the uncertain state of its output when a signal of "1" appears on both inputs R and S. The same is trying to do our neuronal JK latch. To cope with the state of uncertainty at the output when a "0" appears on both inputs, a reset signal combination of "1" on J and "0" on K must be applied first. Besides the neuronal NOR gates of the RS flip-flop, two neuronal AND gates were added, binding the inputs and outputs, as it is described in the theory [8]. The test schematic for the JK neuronal latch is given in Fig. 4. Fig. 5 and Fig. 6 shows the signal diagrams for the simulation with J!=K and J=K.

The signal voltage supplies used in simulations are practically identical with those used for the RS latch simulation, except the V2s signal, whose purpose is to reset the JK latch before the simulation with the signals in phase. The OR gate is provided in order to combine the signal for reset, resulted from V2s, with the signal for the stimulation of the "J" input obtained with V2c.

2.3. The neuronal D flip-flop

The test circuit schematic for D type flip-flop is given in Fig. 7.

The D type flip-flop can be obtained from a J-K latch by always exciting its J and K inputs in opposite phase and having a clock command signal. the command circuit necessary to obtain two neuronal pulses trains in opposite phases is observed. As in the case of the previous test circuits schematics it needs a command voltage supply V2 for the carrier and a voltage signal supply V4 for the envelope combined with an AND gate to create the command signal "D". The carrier signal from V2, combined with an AND gate having an envelope signal from the voltage signal

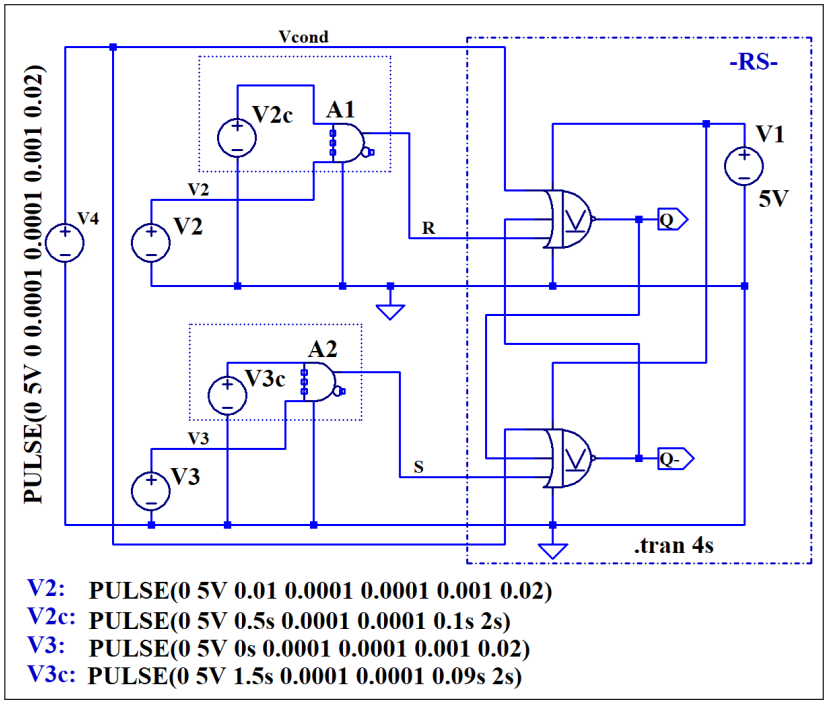

Fig. 2. Neuronal RS latch test circuit schematic.

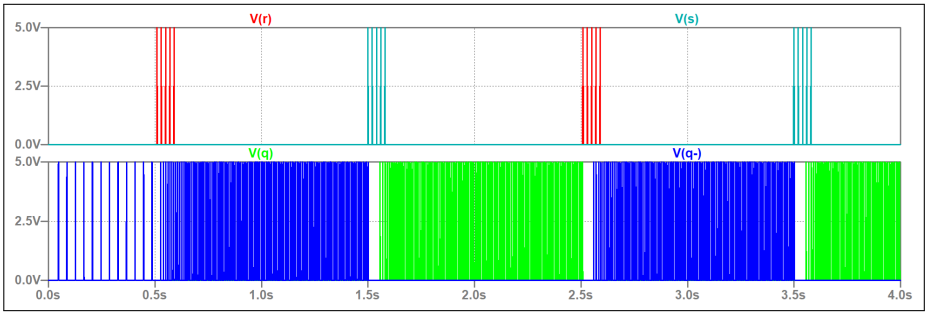

Fig. 3. Signal diagram for neuronal RS latch test circuit schematic.

supply V3, are used to create the clock signal. In addition, a neuronal NOT circuit is required to obtain the inverted signal, "D-", and two neuronal AND gates to combine the "D" signal and the inverted "D-" signal, with the clock signal. In Fig. 8, the signal diagram illustrates the relation between the output and the combination between the D-signal and the clock signal. After a delay of 0.4sec appears the first clock signal which combined with the "D-" input resets the "Q" output.

2.4. The neuronal T latch

A test circuit schematic of the neuronal T latch is given in Fig. 9.

The T latch can also be obtained from a JK latch. Both inputs of the JK latch are bounded together into a single one, "T", that brings a change of the "Q" output when a short pulses train appears at it. The signal diagram for the neuronal T latch is given in Fig. 10.

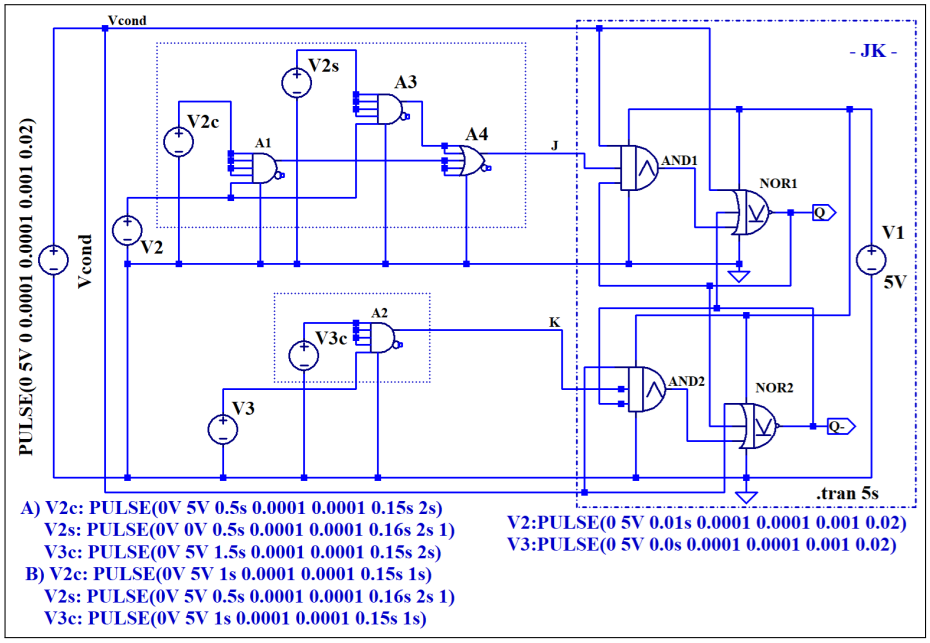

Fig. 4. Neuronal JK latch test circuit schematic.

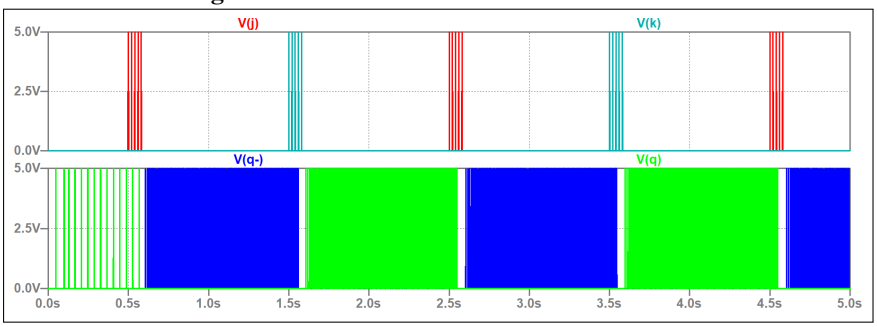

Fig. 5. Signal diagram for neuronal JK latch test circuit schematic with J and K inputs activated alternately.

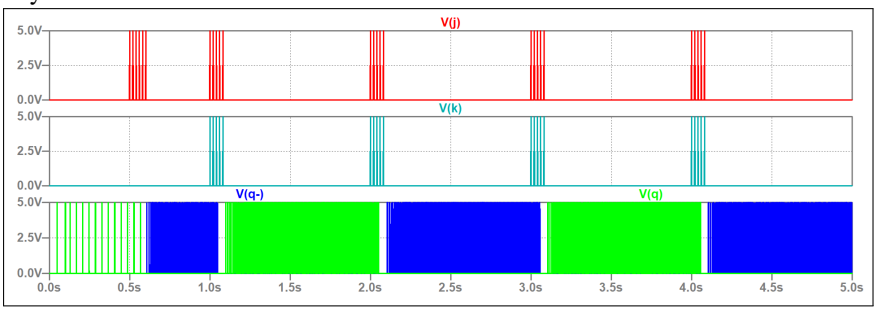

Fig. 6. Signal diagram for neuronal JK latch test circuit schematic with J and K inputs active simultaneously.

3. Implementation and Discussions

In Fig. 11 is given the symbol and block schematic for an α-motoneuronal pair and their Renshaw interneurons for recurrent inhibition controlling agonist/antagonist muscles of a limb.

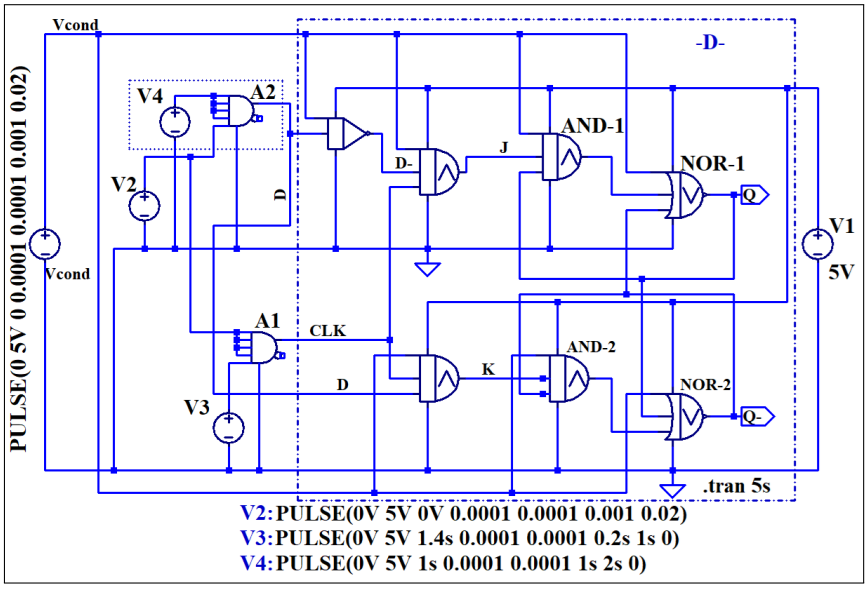

Fig. 7. Neuronal D flip-flop test circuit schematic.

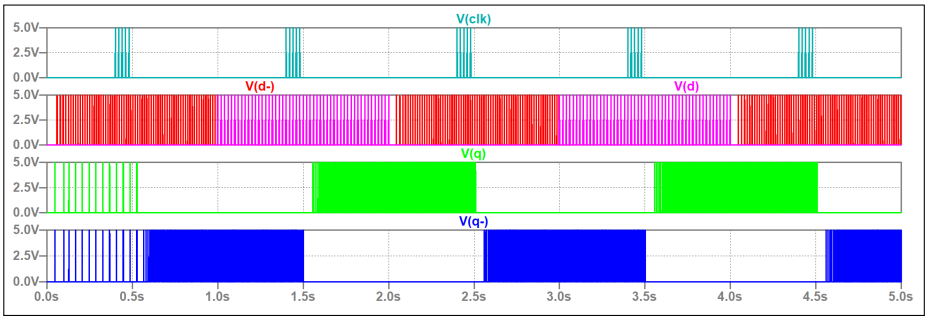

Fig. 8. Signal diagram for neuronal D flip-flop test circuit schematic.

The output of every α-motoneuron runs by a facilitatory synapse in the input of a Renshaw interneuron for its own recurrent inhibition and the inhibition of the opposite α-motoneuron. At the same time the system input of an α-motoneuron excites it with a facilitatory synapse and the opposite α-motoneuron with an inhibitory synapse. The excitation on the inputs "In1" and "In2" can be made using the outputs "Q" and "Q-" of a "T-latch" excited like in the discussion from section 2. In Fig. 12 is given the simulation schematic for the circuit in Fig. 11 and in Fig. 13 the resulted test diagram.

The characteristics of voltage signal supplies is given below under the circuit except the "Cond" voltage signal supply. The circuit from Fig. 9 that is delimited with dashed line is declared as the "T-latch" block in simulations and then it is used in the schematic from Fig. 12.

When the signal is zero on one input, its output is not zero because of the "Cond" signal. This is correct because a muscle has always a minimum excitation. The voltage supply for neuronal circuits is now 5V DC, but further optimizations can be achieved in the future, by decreasing the supply voltage to 1.3V and signal levels to values of 0.1V by replacing the integrated comparator with transistors and by adjusting the transistors parameters. At this moment we considered to design circuits that have the input/output signal shape and behavior similar to those of the

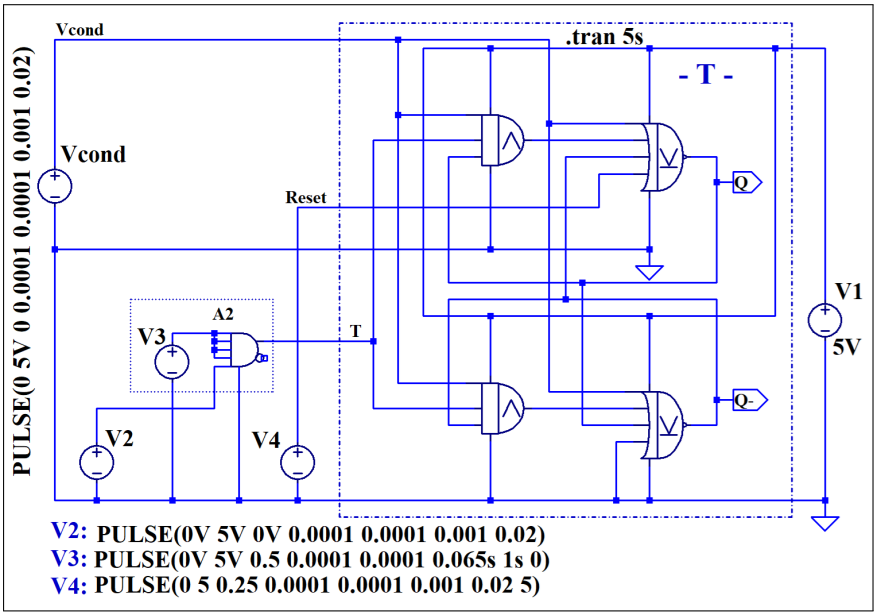

Fig. 9. Test circuit schematic for neuronal T latch.

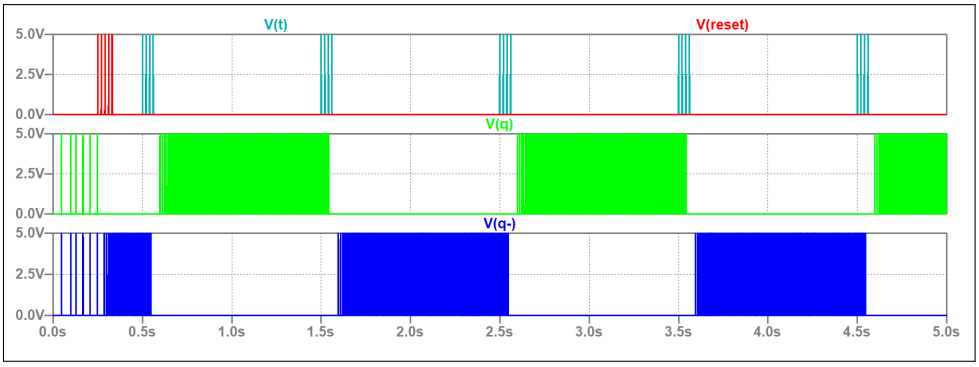

Fig. 10. Signal diagram for neuronal T latch test circuit schematic.

neurons. The simulations presented are useful to understand what is happening at the cellular level of nervous system. It's an improvement of some our previous published papers, from the neuronal block design point of view [8]. An necessary insight into the MOSFET behavior gave us the study of other papers [9]. In fact, there are in vivo experiments that are using signal voltage supplies and excitation signals frequencies and levels similar with those presented by these neuronal blocks [10]. Even not mentioned, the study of some papers in the references list was necessary in order to improve our knowledge in the domain being important to learn firstly from the experience of others. Due to the limited frequencies of [0 .. 100] pulses/sec, linearity can be a problem even for biological circuits communicating by pulses trains. At the spinal cord level, this problem is solved by the organization of neurons like neuronal pools, filtering the neuronal signal, due to their large number and different sizes [2]. In actual simulations this is approached in a global manner. The components values used for the "Neuron" block implementation from Fig. 1 are given in Table 1. Each value is obtained by a preliminary calculus and then opti-

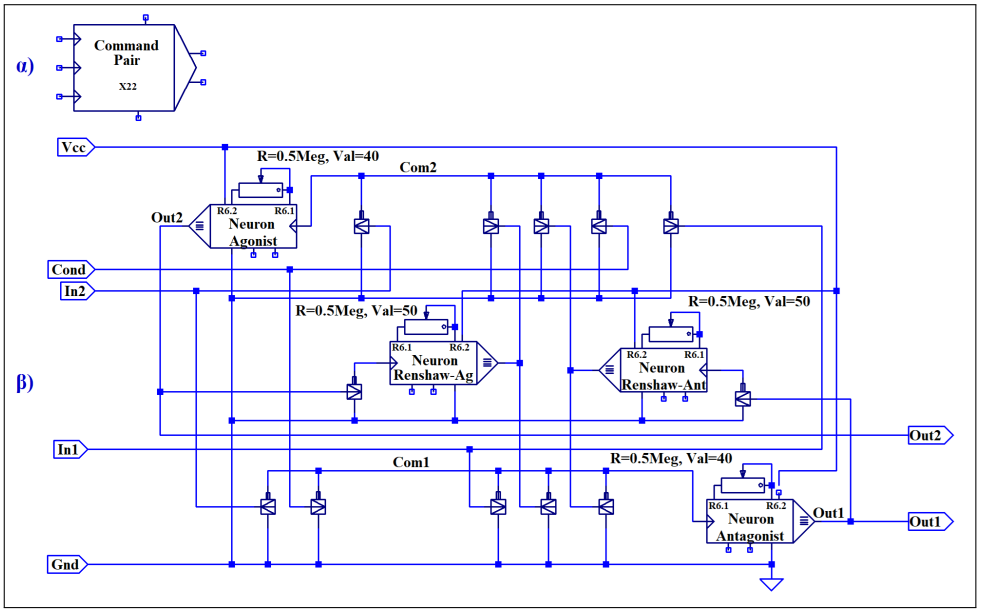

Fig. 11. Circuit symbol α) and schematic β) for an α-motoneuronal pair controlling the agonist-antagonist muscles of a limb.

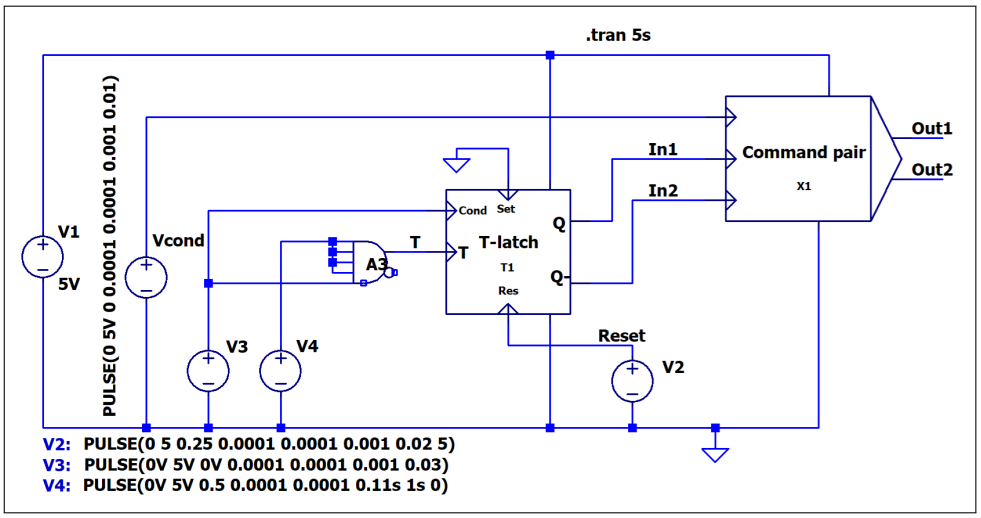

Fig. 12. Test circuit for an α-motoneurons pair of the agonist-antagonist muscles of a limb.

mized by experiments. The Spice parameters for the used MOS transistors are presented in Table 2. These parameters are selected to match the biological signals from [10] with the simulated voltages from our flip-flops as much as possible. The constants formula applied for Fig. 1 are:

$$V_{+(U_1 Out=0V)} = \frac{5(R_1 R_7)}{(R_1(R_5+R_7)+R_2(R_1+R_5+R_7))}. \tag{1}$$

$$V_{+(U_1 Out=5V)} = \frac{5(R_1 R_7+R_1 R_5+R_2 R_5+R_1 R_2)}{((R_1+R_2)(R_5+R_7)+R_1 R_2)}. \tag{2}$$

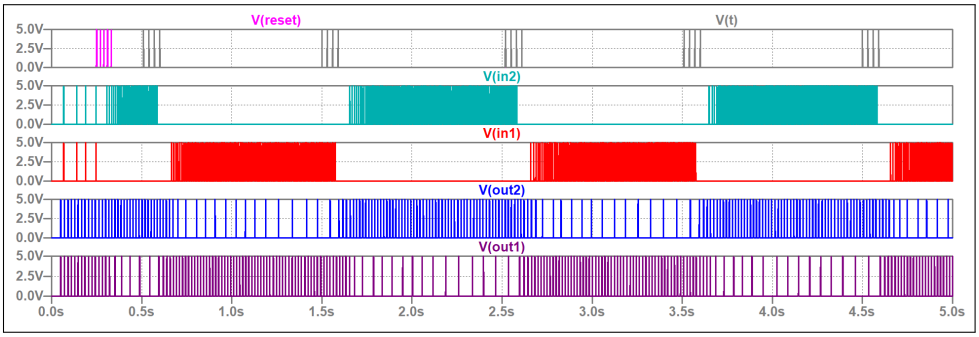

Fig. 13. Test circuit diagram for an α-motoneurons pair of the agonist-antagonist muscles of a limb.

$$\tau_1 = R_{synapse}C_1; \tau_2 = (R_{synapse} + R_4 + R_6)C_2; \tau_3 = R_8C_2; \tau_4 = (R_4 + R_6)\frac{C_1C_2}{C_1 + C_2}; \quad (3)$$

The output frequency depends mainly on the time constants τ1, τ2, τ3, τ4 and at the same time on the difference between voltage levels on input "+" of U1. Rsynapse is the equivalent output resistance of all the inhibitory and facilitatory synapses connected at the terminal "In".

Table 1. Passive components parameters

R1	R2	R3	R4	R5	R7	R8	R9	R10	R11	R12	R14	C1	C2
100k	450k	1M	50k	12.5k	350k	12.5k	175k	15k	1k	10k	100k	1.5μ	67n

Table 2. Main MOSFET parameters used in simulations

MOSFET	Type	Vt0 (V)	Kp (A/V^2)	Lambda (V^{-1})	Ron (mΩ)	Gate (nC)	Vds (V)
Si3460DV	NMOS	1	100	0.01	30	14	20
Si4451DY	PMOS	0.8	90	0.02	10	81	-12

4. Conclusions

This paper extended the neuronal modeling from 0-order to 1-st and 2-nd order digital circuits. Starting from the previous neuronal models, we associated some blocks to latches and flip-flops. As a first latches application, this paper presents the simulation of an α-motoneurons pair stimulated to command an agonist-antagonist muscular pair. Then the paper presents an alternative for the information storage within the central nervous system, knowing that every D latch or flip-flop can be used directly to memorize a bit of information.

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