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Design Space Exploration of Current-Starved Ring Oscillators Based on Graphene Nanoribbons

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Abstract. Graphene is well-suited for ultra-low-power (ULP) nano-electronics due to its exceptional characteristics like ballistic transport and its ability to engineer structures featuring a geometry-induced bandgap. Identifying the conditions necessary for achieving the maximum level of performance and of power-efficiency frequently requires a design space exploration (DSE). By means of calibration and external regulation of the supply voltage, the ULP graphene-nanoribbon (GNR) ring oscillator presented in this paper is capable of exceeding the performance of its $7\,\mathrm{nm}$ FinFET counterpart both in terms of maximum frequency and of power-efficiency. Under nominal supply voltage conditions we achieve a $1.89\times$ higher output frequency while simultaneously reducing the power consumption by $553.8\times$ and achieving a $812\times$ higher power efficiency. After performing a DSE and leveraging both externally-applied supply voltage modulation and output frequency calibration we achieved a $4.81\times$ higher maximum output frequency operation mode and a $242\times$ higher maximum power-efficiency operation mode when configuring both blocks for peak performance for each mode.

Key-words: Current-starved; design space exploration; GNR; graphene; ring oscillator.

1. Introduction

In the current technological environment, which is defined by the integration of CMOS and emerging technologies for portable ultra-low-power electronic devices, there is a continuous ef-

fort to assess the advantages of transitioning from power-intensive, robust, and resilient CMOS-based circuits to the energy-efficient emerging technology alternatives.

Graphene has emerged as a highly promising material for ultra-low-power nano-electronics, owing to its exceptional characteristics such as ballistic transport, flexibility [1], and bio compatibility [2]. These unique properties have spurred the exploration of graphene nanoribbons (GNR) based Boolean logic gates [3, 4] together with synapses [5, 6], McCulloch-Pitts [7] and spiking neurons [8, 9]. In [3], a comparative analysis was conducted between GNR-based logic gates (GNR-L) and $7\,\mathrm{nm}$ FinFET CMOS counterparts. Simulation results show that GNR-L offers two orders of magnitude lower power consumption, six times lower propagation delay, and two orders of magnitude active area reduction. Moreover, [10] proposed a GNR-based 5-bit DAC achieving comparable INL and DNL performance to that of the FinFET variant, i.e., DNL of [-0.196, 0.088] LSB and INL of [-0.809, 0.364] LSB, while operating at only $0.2\,\mathrm{V}$.

The existence of a clock source is necessary both in the digital domain, i.e. clock source for the CPU, implementing timers, memory access, etc., as well as in the analog domain for A/D and D/A data converters, PLLs, monitoring process variation etc. Ring oscillators are favored for their ability to provide a wide tuning range, compact layout, fast startup, and the versatility to generate multiple phases simultaneously [11].

In this paper, we build upon the current source developed in [10] and the GNR structures developed in [7] to design and implement an ultra-low-power GNR-based current-starved oscillator. When supplied at $0.2\,\mathrm{V}$, the GNR oscillator exhibits a power consumption of less than $1\,\mu\mathrm{W}$ at a maximum frequency of $88.4\,\mathrm{GHz}$. We then leverage the investigations for nominal supply voltage operation performed in [12]. By contrast with classical CMOS ring oscillator implementations, determining the propagation delay which characterizes a stage requires us to determine the value of the quantum capacitance associated with the graphene layer in addition to the well understood insulator capacitance of the backgate. The calculation of the quantum capacitance was integrated in the existing conductance computation algorithm and returns a capacitance value which accounts for both the GNR device's geometry as well as the bias conditions it is subjected to for each individual timestep of the simulation.

Our simulation results after accounting for both these capacitances indicate three orders of magnitude lower power consumption for the GNR design when compared with a $7\,\mathrm{nm}$ FinFET counterpart.

The rest of this paper has the following structure: Section 2. presents an overview of related work on graphene, GNR conductance computation, GNR simulation methodology, logic circuits using GNRs, and current-starved oscillators. Section 3. describes the GNR-based current-starved oscillator concept. Section 4. presents the results of our simulations for the GNR and FinFET oscillators and compares their performance. Finally, the paper ends with some concluding remarks in Section 5..

2. Background

Graphene is a two-dimensional (2D) allotrope of carbon whose carbon atoms are arranged in a hexagonal lattice within a single atomic layer. We may visualize graphene's electron structure beginning from carbon's ground-state electron configuration $1s^2 2s^2 2p^2$ with the four outer-shell electrons being its valence electrons. Each carbon atom undergoes sp^2 hybridization leading to three equivalent sp^2 hybrid orbitals and a $2p_z$ orbital [13]. The resulting hybrid sp^2 orbitals

are found in the plane of the graphene sheet and by overlapping with the sp^2 orbitals of their three neighboring carbon atoms form the covalent σ bonds of the graphene lattice. Lastly, the $2p_z$ orbital, which is perpendicular to the graphene sheet's plane overlaps with the $2p_z$ orbitals of neighboring atoms constituting a delocalized π-system and resulting in graphene's extremely high conductivity.

2.1. Electronic properties of graphene

The electronic properties of graphene change as more layers are stacked, exhibiting bulk graphite behavior for large numbers of stacked layers. Single-layer graphene is of special interest, because it is a zero-gap semiconductor with a linear, Dirac-like, spectrum near the Fermi energy [14]. This linear spectrum leads to the formation of quasiparticles that follow the Dirac equation [15], behaving as massless particles with an effective speed equal to the Fermi velocity [16]. In literature these quasiparticles are also known as massless Dirac fermions [17]. Given graphene's Fermi velocity of about $v_F = 10^6\ \mathrm{m/s}$ and it's Dirac-like spectrum, it exhibits high electron mobility and conductivity [18].
High-quality graphene has extremely high intrinsic mobility. Measurements of graphene carrier mobility on SiO_2 substrates show mobilities between $1.5{\times}10^4\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ to $4{\times}10^4\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ at carrier densities of $1 \times 10^{12}\ \mathrm{cm^{-2}}$ [19]. This value is comparable to that of InSb, the inorganic semiconductor with the highest known mobility of $7.7 \times 10^4\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$.

2.2. Graphene nanoribbons (GNRs)

Graphene nanoribbons (GNRs) are open-edged pieces of monolayer graphene whose electronic properties are dictated by their edge geometry [14]. As a consequence of this strong dependence on edge structure, GNRs are classified into two main subtypes: armchair-edge (AGNRs) and zigzag-edge (ZGNRs), with more complex edge geometries being covered in detail in [20]. Additionally, AGNRs exhibit an inverse relationship between geometrically-induced bandgap size and ribbon width [17]. This confinement gap has been experimentally demonstrated in [21] confirming our ability to tune the bandgap by adjusting the ribbon's geometry. The explanation behind this phenomenon is graphene's confinement gap, which, because of its linear spectrum and high Fermi velocity, is significantly larger than in conventional semiconductors [22].

2.3. Graphene state-of-the-art fabrication technology

Graphene fabrication follows two main approaches: top-down and bottom-up. Top-down methods break down bulk graphite but comes as the price of edge roughness [14]. By contrast, bottom-up techniques build graphene from molecular precursors, enabling atomically precise edges and customizable geometries [23].

Top-down synthesis involve breaking down bulk materials into nanoscale graphene structures. Micromechanical exfoliation, also known as the 'Scotch tape' method, produces high-quality graphene but is impractical for large-scale production [24]. Alternatively, carbide decomposition enables graphene growth on SiC surfaces, where a buffer layer forms and preserves graphene's properties [25]. Another method involves squashing carbon nanotubes to create

graphene nanoribbons (GNRs) with smooth edges, achieving sub-$10\,\mathrm{nm}$ device fabrication [26]. Electron beam lithography (EBL) is also used to pattern narrow GNRs with confinement-induced band gaps, with resolutions improving to sub-$10\,\mathrm{nm}$ [27].

Bottom-up synthesis build graphene structures from molecular precursors. Chemical vapor deposition (CVD) grows large-area graphene films on metal substrates such as Cu and Ni, enabling scalable production and easy transfer to other substrates [28]. Another precise method uses molecular precursors to synthesize atomically defined GNRs, allowing for controlled edge structures and electronic properties [29].

2.4. GNR based devices

Configuring the geometrical parameters of the generic non-rectangular GNR-based device, illustrated in Figure 1, allows us to induce a bandgap and achieve various analog behaviors.

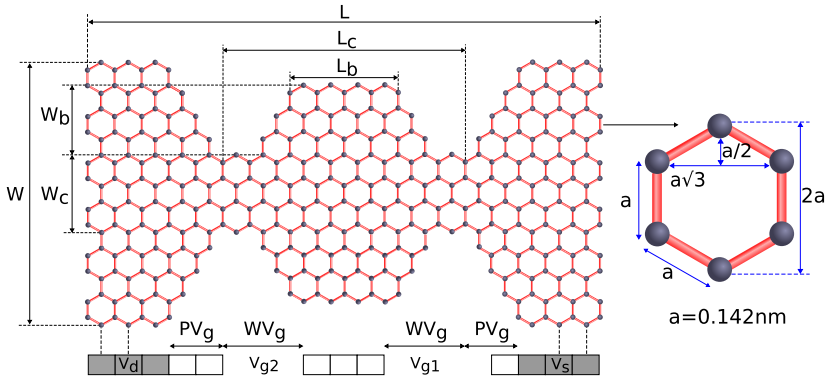
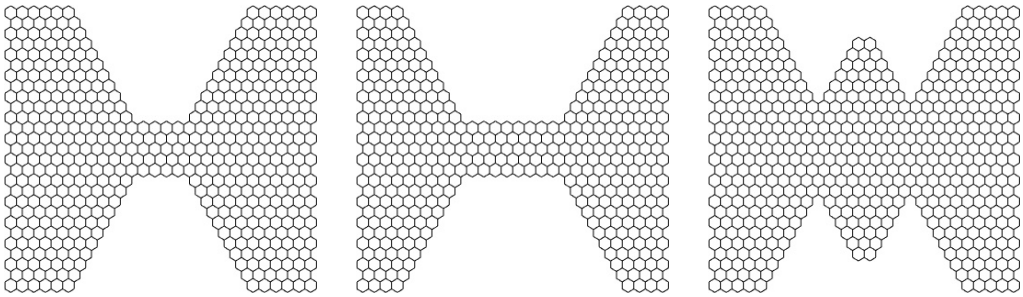


Fig. 1. GNR Geometry Description Parameters [30].

A set of three GNR geometries, capable of fulfilling the roles of current source and low-side and high-side switches [7] is illustrated in Figure 2. The exact structure geometries, identified through iterative conductance map plot evaluations [3], are detailed in Table 1.



(a) GNR_{ISRC} (b) GNR_{DOWN} (c) GNR_{UP}

Fig. 2. Graphene-based device topologies.

Table 1. Dimensions of GNR structures [7]

	(W,L)	(W_c,L_c)	(W_b, L_b)	(P_{V_G}, W_{V_G})
GNR_{ISRC}	$(41, 27\sqrt{3})$	$(8, 4\sqrt{3})$	$(0, 0)$	$(2\sqrt{3}, 6\sqrt{3})$
GNR_{UP}	$(41, 27\sqrt{3})$	$(14, 8\sqrt{3})$	$(9, 2\sqrt{3})$	$(12\sqrt{3}, 6\sqrt{3})$
GNR_{DOWN}	$(41, 27\sqrt{3})$	$(8, 8\sqrt{3})$	$(0, 0)$	$(3\sqrt{3}, 6\sqrt{3})$

2.5. Simulation framework

The assessment of the GNR-based circuits is conducted using a hybrid simulation framework that combines Cadence Spectre's mixed-signal environment with Matlab's parallel computing toolbox. This co-simulation methodology enables SPICE-level circuit simulations alongside precise atomistic-level GNR computations in Matlab.

To calculate the electronic transport properties of GNRs, we use the tight-binding Hamiltonian approach to characterize their structure. Additionally, the Non-Equilibrium Green Function (NEGF) quantum transport model is applied to solve the Schrödinger equation and, using the Landauer formalism, compute the GNRs' conductance [31] using Equation 1.

$$G = \frac{q \cdot \int_{-\infty}^{+\infty} T(E) \cdot (f_0(E-\mu_1) - f_0(E-\mu_2))dE}{h \cdot (V_d - V_s)}, \tag{1}$$

where q is the electron charge, h is the Planck constant, $T(E)$ is the transmission function, $f_0(E)$ is the Fermi-Dirac distribution function at temperature T, and $\mu_{1,2}$ denote the Fermi energy of the source and drain contacts.

In addition, the back-gate's insulator capacitance, C_{ins}, and the graphene's quantum capacitance, C_{ins}, should be determined to generate accurate transient simulation results.

The insulator capacitance, C_{ins}, can be modelled using the fundamental parallel plate capacitor equation where we provide the equivalent permittivity μ_{eq}, the oxide thickness, t_{ox}, and the area of the GNR device, A_{gnr}.

The quantum capacitance, C_q, is then calculated using Equation 2 by integrating the product of the density of states, $DOS(E)$, and the thermal broadening function, $F_T(E)$, over all energy levels E [32]. This determines the quantum capacitance based on the distribution of energy states.

$$C_q = q^2 \int_{-\infty}^{+\infty} \mathrm{DOS}(E) \cdot F_T(E - (\mu_1 - \mu_2))\, dE \tag{2}$$

2.6. Ring oscillators

Given the most rudimentary ring oscillator, the frequency f can be determined knowing the number of stages N, and the propagation delay of each stage t_d using Equation 3. Furthermore, if the load capacitance of the inverter, C_L, the activity factor, α, and the supply voltage, V_{supply}, are known, then we can approximate the power consumption of the circuit using Equation 4.

$$f = \frac{1}{2 \cdot N \cdot t_d} \tag{3}$$

$$P = \alpha \cdot N \cdot C_L \cdot V_{supply}^2 \cdot f \tag{4}$$

The main drawback of this implementation is the variability induced by t_d into the oscillation frequency, which will vary linearly with V_{supply} and non-linearly through drain currents I_{PMOS} and I_{NMOS} against process, temperature and V_{supply} variations, as shown in Equation 5.

$$t_d \approx \ln(2) \cdot \frac{C_L \cdot V_{supply}}{2} \cdot \left(\frac{1}{I_{PMOS} + I_{NMOS}} \right) \tag{5}$$

The propagation time variability can be partially mitigated using the current starving technique. This works by enforcing a maximum current, I_{bias}, through the inverter's transistors by adding a current source in series and yields Equation 6. Equation 4 remains applicable for calculating power consumption.

$$f = \frac{I_{bias}}{2 \cdot N \cdot C_L \cdot V_{supply}} \tag{6}$$

3. Designing a GNR-based Current-starved Ring Oscillator

In this section we present the proposed GNR-based and FinFET current-starved ring oscillator and outline the necessity of performing a design space exploration (DSE) in the context of single-ended ring oscillator supply voltage sensitivity.

3.1. GNR-based and FinFET oscillator stage

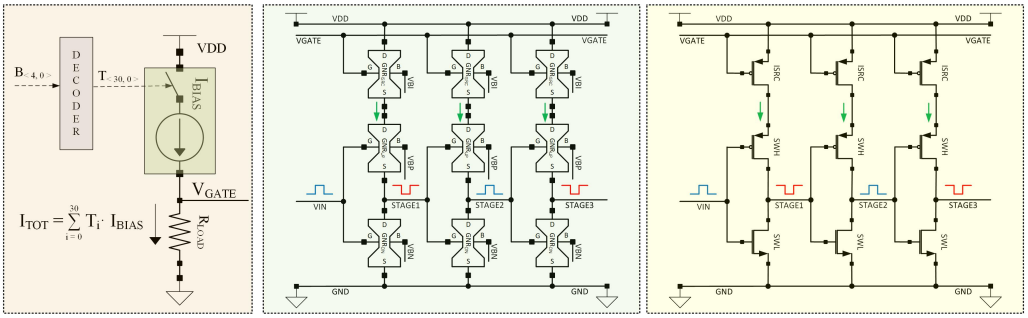


Fig. 3. a) 5-bit DAC (left) for frequency tuning b) GNR-based (middle) and FinFET (right) ring oscillator sections.

The implementations of the ring oscillator stages using GNR-based devices and FinFETs together with a 5-bit DAC used for frequency tuning are depicted in Figure 3.

The reason for the DAC's presence is the lack of an $180°$ phase-shift at low frequency for signals propagating from the $gate$ to the $drain$ terminal of the GNR device shown in Figure 2a. An immediate consequence is that a classic current mirror configuration cannot be used to implement a current source.

To overcome this limitation we propose modulating the current through the GNR device by driving its gate using the output voltage of the previously developed 5-bit DAC [10].

By contrast, a classic current mirror could be used for the FinFET implementation, but the granularity provided by the already implemented 5-bit FinFET DAC is sufficient for trimming the ring oscillator's frequency. Moreover, while a current mirror can achieve very high mirroring precision in CMOS, deep sub-micron devices provide weak output resistance that negates the advantage of using mirrors.

To avoid doubling the device count of the proposed design, we chose to apply current starving only to the high side of the inverter. The absence of an NMOS current source equivalent on the low side of the inverter stages will result in the overall propagation delay (t_d) being primarily influenced by the I_{PMOS} term during the rising edge of the output signal. This will be complemented by a rapid falling edge of negligible duration generated by the I_{NMOS} term.

A disadvantage of using a current DAC to configure the ring oscillator is the quiescent current consumption of the active current sources which reaches a maximum of $31 \cdot I_{bias}$ for the maximum DAC input code. This quiescent current can be eliminated by adding a storage capacitor for sampling the analog value applied to V_{gate} and disconnecting it with a GNR device similar to that used for the access transistors in the GNR-based SRAM presented in [3].

3.2. GNR current-starved ring oscillator

The complete implementation of the GNR-based current-starved ring oscillator is shown in Figure 4 and is comprised of 8 inverter-like stages. The last $180°$ phase shift is ensured by a GNR NAND gate which constitutes the circuit's enable. The oscillator's frequency can be modulated by adjusting the current DAC input code, which, in turn, regulates the gate voltage of the current source device.

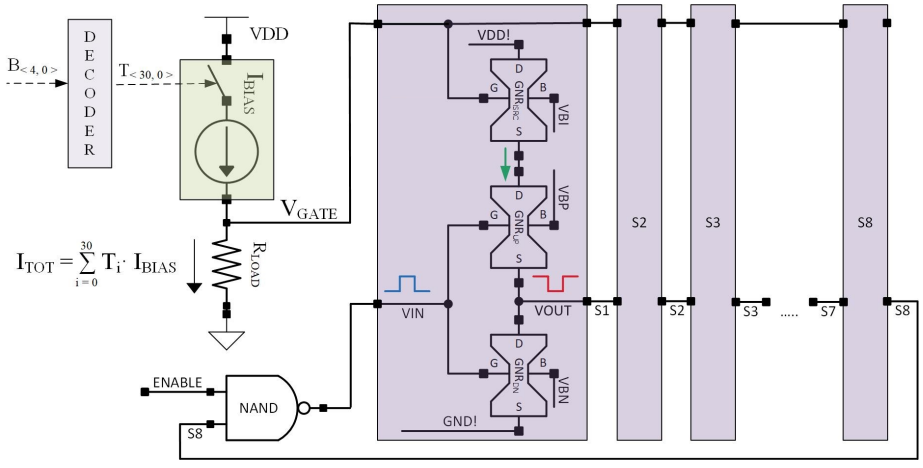


Fig. 4. GNR-based current-starved ring oscillator.

3.3. Design space exploration of ring oscillator supply voltage sensitivity

One critical factor which impacts the accuracy of the output frequency is the oscillator's supply voltage sensitivity. Certain topologies, such as differential ring oscillators, provide an increased level of resilience to variations of the supply voltage [11]. By contrast, classical single-ended ring oscillators are highly sensitive to the variation of the supply voltage, because supply variations translate into changes of the individual oscillator stage thresholds.

Given that we propose a single-ended implementation, we are interested in establishing the impact of supply voltage variations on the oscillator's performance by means of a design space exploration (DSE).

Ring oscillators are known [11] to be sensitive to variations of the supply voltage, as captured in Equation 6. Considering the voltage DAC frequency calibration strategy employed, we cannot perform a simple 1D sweep of the supply voltage while simultaneously maintaining a fixed DAC input code, because the DAC's output voltage would also scale with the supply voltage and apply a varying overdrive voltage to the current source devices. Instead, to provide a complete image of the supply sensitivity of the two oscillator implementations, we must perform a 2D design space exploration (DSE) to identify the output frequency and the power efficiency's sensitivity to the supply voltage VDD and the DAC input code.

4. Simulation Results

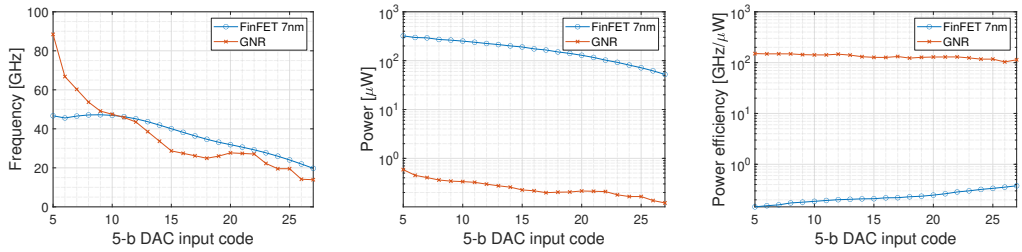
The simulation framework outlined in 2.5. was utilized to assess the performance of the proposed GNR-based current-starved oscillator, while SPICE simulations were employed to evaluate the operation of the FinFET-based counterpart.

4.1. GNR vs. FinFET oscillator performance at nominal supply voltage

The simulation results obtained for the GNR-based and FinFET ring oscillators are compared in terms of frequency range, power consumption, and power efficiency. The variation of these three parameters with the DAC's input code is presented in Figure 5. The simulations presented in this subsection were performed at the nominal supply voltage of both technologies, i.e., $0.2\,\mathrm{V}$ for GNR-based devices and $0.8\,\mathrm{V}$ for $7\,\mathrm{nm}$ FinFET devices.

The code range applied at the input of the DAC is intentionally limited, given that for the lower range of V_{gate} voltages the FinFET PMOS device would enter the linear region and compromise current starving. Similarly, the upper range of V_{gate} would cause the device to enter the cut-off region.

Reviewing the results from Table 2, we observe that the oscillation frequencies of the GNR-based and $7\,\mathrm{nm}$ FinFET-based ring oscillator implementations are closely matched. This resemblance can be attributed primarily to the relatively low $1.2\,\mu\mathrm{A}$ current flowing through the GNR device. When comparing the GNR-based and $7\,\mathrm{nm}$ FinFET-based implementations, the GNR starved ring oscillator demonstrates significantly lower power consumption, nearly three orders of magnitude less, thanks to its smaller parasitic capacitances. This leads to nearly three orders of magnitude superior power efficiency despite similar oscillation frequencies.



(a) $Frequency$ (b) $Power$ (c) $Power\ efficiency$

Fig. 5. Performance comparison of GNR-based and 7 nm FinFET ring oscillators: a) frequency, b) power, c) power efficiency.

Table 2. GNR-based vs. FinFET ring oscillator results

	Frequency [GHz]	Power consumption [μW]	Power efficiency [GHz/μW]
FinFET	19.7 - 46.7	52.2 - 321.2	0.14 - 0.40
GNR	13.9 - 88.4	0.12 - 0.58	113.7 - 150.4

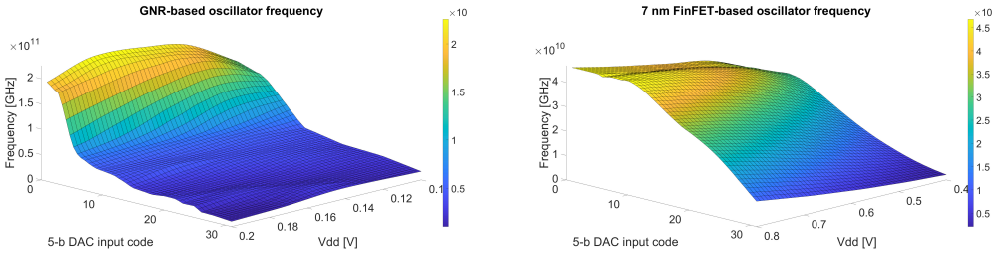
4.2. Design space exploration of GNR and FinFET oscillators

Figure 6 presents the design space exploration (DSE) of the oscillators' output frequency as a function of the supply voltage and the 5-bit DAC input code. We begin by analyzing the frequency characteristics of the GNR-based oscillator, as shown in Figure 6a. The plot can be divided into three distinct regions based on the DAC input code: a) the high-code region (10-31) where frequency varies slowly, b) the transition region (3-10) where frequency changes steeply, and c) the low-code region (0-3) where the frequency variation slows down again. In the high-code and transition region the frequency variation profile is attributed to the I_{ds} characteristic of the GNR current source device illustrated in [7]. In the low-code region the current source no longer limits the current drawn by the inverters, resulting in a nearly constant frequency with respect to the DAC code.

Analyzing the same plot as a function of the supply voltage V_{DD}, we observe that the maximum oscillation frequency occurs at approximately $0.15\,\mathrm{V}$, while the frequency decreases at both the lower boundary ($0.1\,\mathrm{V}$) and the upper boundary ($0.2\,\mathrm{V}$). The decline at low V_{DD} can be attributed to the I_{ds} characteristic of the GNR current source device, as the device exits its saturation-like region, leading to a reduction in I_{bias}. Conversely, the frequency drop at high V_{DD} aligns with the prediction from Equation 6, since I_{bias} remains constant while V_{supply} increases.

Compared with the frequency characteristic of the 7 nm FinFET implementation we observe that the GNR-based implementation achieves a higher maximum frequency, but the variation of the frequency across the DAC calibration range has a pronounced non-linear characteristic.

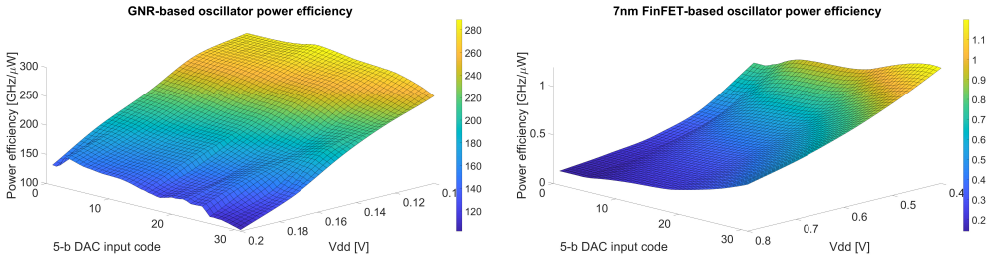
Figure 7 presents the design space exploration (DSE) of the oscillators' power-efficiency as a function of the supply voltage and the 5-bit DAC input code. We begin by analyzing the results for the GNR-based oscillator, as shown in Figure 7a. When sweeping the DAC calibration



(a) GNR output frequency (b) FinFET output frequency

Fig. 6. Output frequency DSE of GNR-based and 7 nm FinFET.

code there is little influence on the power-efficiency, because the steep frequency increase seen in Figure 6a cancels out the increased power consumption. However, sweeping the supply voltage reveals that decreasing the supply voltage ensures a monotonic increase of the power-efficiency. Looking at the results for the FinFET-based oscillator, shown in Figure 7b we see a slight decrease in the power efficiency at low-code range, which can be correlated with the plateau of the oscillator's frequency seen in Figure 6b. Similarly with the GNR-based implementation, we see a monotonically improved power-efficiency low supply voltages.



(a) GNR power-efficiency (b) FinFET power-efficiency

Fig. 7. Power-efficiency DSE of GNR-based and 7 nm FinFET.

A summary of the results from the output frequency DSE from Figure 6 is provided in Table 3. Similarly, a summary of the key finding from the power-efficiency DSE from Figure 7 is provided in Table 4.

Table 3. GNR-based vs. FinFET ring oscillator output frequency DSE

	Supply Voltage [V]	DAC code [−]	Max. Frequency [GHz]
FinFET	0.8	0	46.90
GNR	0.175	0	225.54

Table 4. GNR-based vs. FinFET ring oscillator power-efficiency DSE

	Supply Voltage [V]	DAC code [−]	Max. Power efficiency [GHz/μW]
FinFET	0.4	31	1.191
GNR	0.1	12	288.80

5. Conclusions

In this paper, we investigated the potential of GNR devices to implement high-frequency ultra-low-power internal oscillators for multi-technology ICs. We explored the frequency range over which we can tune the oscillator by driving the gate of the current source GNR-based device. The dynamic power consumption was reduced by applying the current starving technique to the ring oscillator topology. The proposed GNR-based design was compared with a $7\,\mathrm{nm}$ FinFET counterpart and achieved a $1.89\times$ higher output frequency while simultaneously reducing the power consumption by $553.8\times$ and achieving a $812\times$ higher power efficiency. A DSE of the frequency calibration and supply voltage was performed revealed that the GNR-based implementation achieves a $4.81\times$ higher maximum output frequency and a $242\times$ higher maximum power-efficiency when compared with the optimally configured FinFET implementation configured.

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