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A comparison between the G_m based implementations of voltage mode and current mode capacitance multipliers

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Abstract. A comparison between two G_m based implementations of capacitance multipliers, one following a voltage mode perspective and another one following a current mode perspective is performed. The transconductor based circuit solution for voltage mode capacitance multiplication employs the Miller effect around a voltage amplifier implemented as a transconductance amplifier paired with another transconductor acting as a load. The current mode multiplier used as reference in the comparison uses the same components and is built around a typical current mirror by substituting the MOS transistors with transconductance amplifiers. For both structures the ratio of the two transconductances defines the multiplication factor. Due to the transconductance tunability, the multiplication factor is adjustable in a wide range. The results show an important advantage of the voltage mode multiplier with regards to the low frequency behavior in comparison to a current mode G_m-based implementation, recommending the voltage mode circuit for frequency compensation applications. A first order low-pass filter is implemented as an application of the two described architectures using discrete G_m integrated circuits.

Key-words: MOS capacitor; capacitance multiplier; adjustable capacitor; transconductance amplifier.

1. Introduction and preliminary results

Despite the downward trend in the oxide layer thickness along with the development of the CMOS technology, increasing electrical capacitance per unit area cannot keep pace with reducing the minimum size of field effect devices. The benefit for analog integrated circuits (ICs) as a consequence of transistor scaling stems from reduced parasitics that enable high frequency operation or, for similar speed, a lower energy footprint. Yet, in the case of IC passive devices,

scaling offers fewer benefits. Looking to integrate high capacitance values in ICs, analog circuit designers resort to active circuits to multiply the capacitive effect of passive capacitors while keeping a low die area and energy footprint.

Regarding the scaled electrical quantity, one can distinguish two classes of capacitance multipliers: voltage mode multipliers and current mode multipliers [1]. This paper presents a comparison between a G_m based current mode capacitance multiplier and an alternative implementation of the G_m based capacitance multiplier that exhibits voltage mode operation. As the results show, the voltage mode multiplier presents an important advantage with regard to the low frequency behavior in comparison to the current mode G_m-based implementation, recommending the circuit for low frequency small signal applications.

2. The current mode capacitance multiplier

The current scaling principle is illustrated in Fig. 1a. A voltage applied to the structure induces an i_c current through the capacitor. The current-controlled current source (CCCS) generates a K times scaled up replica of this current. Giving the fact that the input current is $(K+1)i_c$, the structure behaves as a $(K+1)$ multiplied capacitor. A simple transistor level implementation, build around a typical current mirror, is shown in Fig. 1b, while the G_m based implementation in Fig. 1c is obtained by replacing the NMOS transistors in Fig. 1b with transconductance amplifiers [2]. A G_m-C implementation of the current mode capacitive multiplier is of great interest given the ubiquity of the transconductance amplifier in the synthesis of analog circuits. Moreover, the multiplication factor of the circuits shown in Fig. 1b and Fig. 1c is given by the ratio of two transconductances, making the control of the equivalent capacitance more flexible.

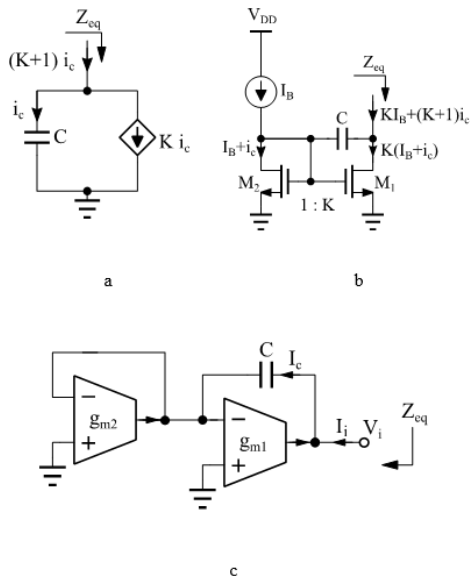

Fig. 1. Current mode capacitance multiplication: (a) principle, (b) transistor level implementation and (c) G_m implementation, [2].

3. The voltage mode capacitance multiplier

The principle of the voltage mode capacitance multiplier is illustrated in Fig. 2a. A current injected into the structure generates a v_c voltage drop across the base capacitor C. The voltage-controlled voltage source (VCVS) produces a voltage such that the voltage drop across the entire structure represents a $(K+1)$ scaled down replica of the voltage across the base capacitor. In this way the structure behaves as a $(K+1)$ multiplied capacitor. Fig. 2b shows the Miller technique applied in the implementation of a voltage mode multiplier.

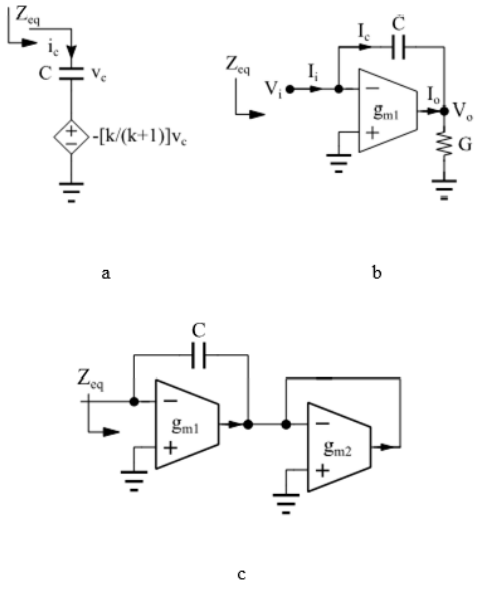

Fig. 2. Voltage mode capacitance multiplication: (a) principle, (b) typical implementation of the multiplier based on the Miller effect and (c) G_m implementation.

A G_m based voltage mode implementation of a capacitance multiplier is presented in [3] and illustrated in Fig. 2c. The main idea of the circuit is to use a transconductance amplifier in order to implement the "G"

4. Frequency analysis considering ideal transconductors

a. Current mode

Considering ideal transconductance amplifiers, the equivalent circuit in Fig. 3 will be used for frequency analysis of the Fig. 1c current mode multiplier:

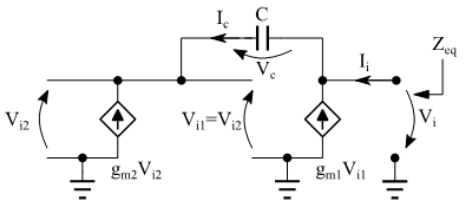

Fig. 3. Equivalent circuit for frequency analysis of the current mode capacitance multiplier by considering ideal transconductors.

One can write:

$$V_i = V_c - V_{i2} = I_c\left(\frac{1}{sC} + \frac{1}{g_{m2}}\right) \tag{1}$$

$$I_i = -\big(g_{m1} + g_{m2}\big)V_{i1} = \big(g_{m1} + g_{m2}\big)\frac{I_c}{g_{m2}} \tag{2}$$

It follows that:

$$Z_{eq} = \frac{V_i}{I_i} = \frac{\frac{1}{sC} + \frac{1}{g_{m2}}}{(g_{m1} + g_{m2})\frac{1}{g_{m2}}} = \frac{1}{g_{m2} + g_{m1}} + \frac{1}{sC\left(1 + \frac{g_{m1}}{g_{m2}}\right)} \tag{3}$$

b. Voltage mode

Considering ideal transconductance amplifiers, one can write for the Fig. 2b structure:

$$I_i = I_c = sC(V_i - V_o) \tag{4}$$

$$I_i + I_o - GV_o = 0 \tag{5}$$

$$I_o = -g_{m1}V_i \tag{6}$$

It follows that:

$$sC(V_i - V_o) - g_{m1}V_i - GV_o = 0 \tag{7}$$

$$\frac{V_o}{V_i} = \frac{sC - g_{m1}}{sC + G} \tag{8}$$

The equivalent input impedance of the structure will be:

$$Z_{eq} = \frac{V_i}{I_i} = \frac{V_i}{sC(V_i - V_o)} = \frac{V_i}{sCV_i(1 - \frac{sC - g_{m1}}{sC + G})} = \frac{sC + G}{sC(G + g_{m1})} \tag{9}$$

If the conductance G is implemented using a transconductance amplifier, $G = g_{m2}$, as in Fig. 2c:

$$Z_{eq} = \frac{V_i}{I_i} = \frac{sC}{sC(g_{m2} + g_{m1})} + \frac{g_{m2}}{sC(g_{m2} + g_{m1})} = \frac{1}{g_{m2} + g_{m1}} + \frac{1}{sC(1 + \frac{g_{m1}}{g_{m2}})} \tag{10}$$

Therefore, the equivalent input impedance of both structures shown in Fig. 1c and Fig. 2c is:

$$Z_{eq} = \frac{V_i}{I_i} = \frac{1}{g_{m2} + g_{m1}} + \frac{1}{sC(1 + \frac{g_{m1}}{g_{m2}})} \tag{11}$$

The equivalent model of both structures from Fig. 1c and Fig. 2c is shown in Fig. 4, the equivalent parameters being

$$C_{eq} = C(1 + \frac{g_{m1}}{g_{m2}}) \tag{12}$$

$$R_{eq} = \frac{1}{g_{m2} + g_{m1}} \tag{13}$$

The differences between the structures in Fig. 1c and Fig. 2c can be emphasized by considering the non-ideal effects introduced by the transconductors.

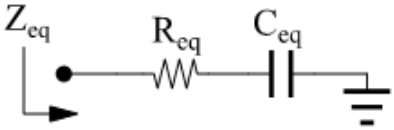

Fig. 4. Linear polarization: (a) vertical (V) and horizontal (H); (b) slant (S) polarization.

5. Frequency analysis considering non-ideal effects

a. Current mode

Considering non-zero output conductances as well as the effect of input and output capacitances, a frequency analysis is carried on for the current mode structure in Fig. 1c, as depicted in [4]. The small signal circuit presented in Fig. 5 is used.

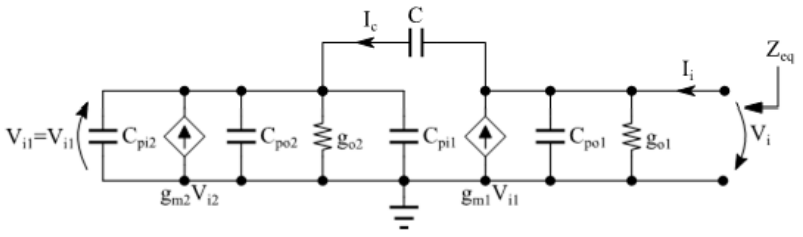

Fig. 5. Equivalent circuit for frequency analysis of the current mode capacitance multiplier by considering non-ideal effects.

Considering the following notation:

$$C_{pi} = C_{pi1} + C_{pi2} + C_{po2} \tag{14}$$

the equivalent circuit for frequency analysis will be simplified as shown in Fig. 6.

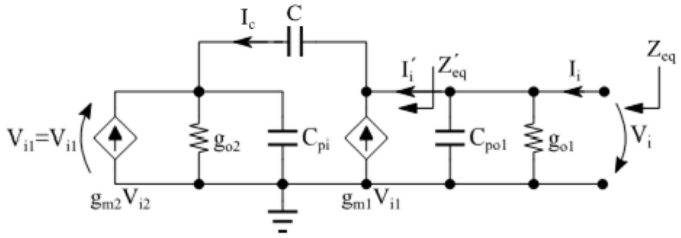

Fig. 6. Simplified equivalent circuit.

The expression of the input impedance will be:

$$Z_{eq} = \frac{V_i}{I_i} = g_{o1} || \frac{1}{sC_{po1}} || Z'_{eq} \tag{15}$$

One can write:

$$I_c = sC(V_{i1} + V_i) \tag{16}$$

$$I'_i + g_{m1}V_{i1} - I_c = 0 \tag{17}$$

$$I_c + g_{m2}V_{i1} + g_{o2}V_{i1} + sC_{pi}V_{i1} = 0 \tag{18}$$

By processing these relations, we get:

$$V_{i1} = -\frac{sC}{s(C + C_{pi}) + g_{m2} + g_{o2}} V_i \tag{19}$$

$$I'_i = V_i \left[sC + \frac{sC(g_{m1} - sC)}{s(C + C_{pi}) + g_{m2} + g_{o2}} \right] \tag{20}$$

The expression of Z'_{eq} will be computed as:

$$Z'_{eq} = \frac{C + C_{pi}}{CC_{pi}} \frac{s + \frac{g_{m2}+g_{o2}}{C+C_{pi}}}{s\left(s + \frac{g_{m1}+g_{m2}+g_{o2}}{C_{pi}}\right)} \tag{21}$$

which can be written as:

$$Z'_{eq} = \frac{C + C_{pi}}{CC_{pi}} \frac{s + \alpha}{s(s + \beta)} \tag{22}$$

where:

$$\alpha = \frac{g_{m2} + g_{o2}}{C + C_{pi}} \tag{23}$$

$$\beta = \frac{g_{m1} + g_{m2} + g_{o2}}{C_{pi}} \tag{24}$$

Using the result:

$$\frac{s+\alpha}{s(s+\beta)} = \frac{1}{\beta}\left(\frac{\alpha}{s} + \frac{\beta-\alpha}{s+\beta}\right) \tag{25}$$

the Z'_{eq} expression becomes:

$$Z'_{eq} = \frac{1}{sC_{ssi}} + \frac{\frac{1}{C_{ppi}}}{s + \frac{1}{C_{ppi}R_{ppi}}} \tag{26}$$

where:

$$C_{ssi} = \left(1 + \frac{g_{m1}}{g_{m2} + g_{o2}}\right)C = (1 + K_i)C \tag{27}$$

$$C_{ppi} = \frac{1}{1 + \frac{g_{m1}}{g_{m1}+g_{m2}+g_{o2}}\frac{C_{pi}}{C}}C_{pi} = \frac{1}{1 + \frac{K_i}{K_i+1}\frac{C_{pi}}{C}}C_{pi} \tag{28}$$

$$R_{ppi} = \frac{1}{g_{m1} + g_{m2} + g_{o2}}\left(1 + \frac{K_i}{K_i + 1}\frac{C_{pi}}{C})\right) \tag{29}$$

The expression of Z'_{eq} (26) shows that the input impedance Z_{eq} corresponds with the circuit in Fig. 7, the parameters being depicted by (27), (28) and (29).

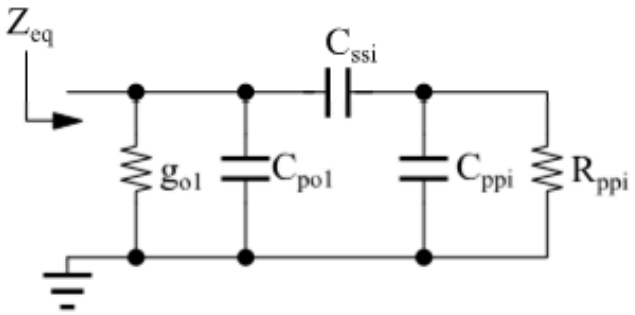

Fig. 7. Input impedance model for the current mode capacitance multiplier [2].

The multiplication factor of the current mode capacitance multiplier is $K_i = g_{m1}/(g_{m2} + g_{o2})$.

In ideal conditions, with $C_{pi1,2} = C_{po1,2} = 0$ and $g_{o1,2} = 0$, the equivalent circuit is reduced to the one in Fig. 4 as emphasized by the relationships (30) and (31):

$$C_{ssi} = C_{eq} = C\left(1 + \frac{g_{m1}}{g_{m2}}\right) \tag{30}$$

$$R_{ppi} = R_{eq} = \frac{1}{g_{m2} + g_{m1}} \tag{31}$$

b. Voltage mode

Considering finite input and output resistances as well as the effect of parasitic capacitors, the small signal circuit presented in Fig. 8 is obtained:

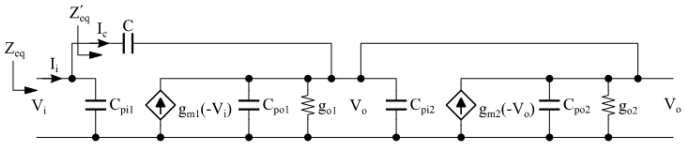

Fig. 8. Equivalent circuit for frequency analysis of the voltage mode capacitance multiplier by considering non-ideal effects.

By considering the following notations:

$$g_o = g_{o1} // g_{o2} \tag{32}$$

$$C_{pv} = C_{po1} + C_{pi2} + C_{po2} \tag{33}$$

the equivalent circuit becomes the one in Fig. 9:

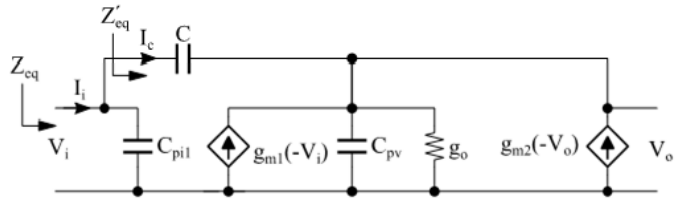

Fig. 9. Simplified equivalent circuit.

Using the equivalent circuit shown in Fig. 9, one can write:

$$Z_{eq} = \frac{V_i}{I_i} = Z'_{eq} || \frac{1}{sC_{pi1}} \tag{34}$$

$$Z_{eq} = \frac{V_i}{I_c} \tag{35}$$

$$I_c = sC(V_i - V_o) \tag{36}$$

$$sC(V_i - V_o) - g_{m1}V_i - g_{m2}V_o - (sC_{pv} + g_o)V_o = 0 \tag{37}$$

It follows that:

$$\frac{V_o}{V_i} = \frac{sC - g_{m1}}{(C + C_{pv}) + g_{m2} + g_o} \tag{38}$$

The equivalent input impedance of the structure will be:

$$Z'_{eq} = \frac{V_i}{I_c} = \frac{V_i}{sC(V_i - V_o)} = \frac{1}{sC\Big(1 - \frac{sC - g_{m1}}{s(C+C_{pv})+g_{m2}+g_o}\Big)} \tag{39}$$

Consequently:

$$Z'_{eq} = \frac{V_i}{I_c} = \frac{s(C + C_{pv}) + g_{m2} + g_o}{sC(sC_{pv} + g_{m1} + g_{m2} + g_o)} = \frac{C + C_{pv}}{CC_{pv}} \frac{s + \frac{g_{m2}+g_o}{C+C_{pv}}}{s(s + \frac{g_{m1}+g_{m2}+g_o}{C_{pv}})} \tag{40}$$

which can be written as:

$$Z'_{eq} = \frac{C + C_{pv}}{CC_{pv}} \frac{s + \alpha}{s(s + \beta)} \tag{41}$$

$$\alpha = \frac{g_{m2} + g_o}{C + C_{pv}} \tag{42}$$

$$\beta = \frac{g_{m1} + g_{m2} + g_o}{C_{pv}} \tag{43}$$

Using the result in (25) the Z'_{eq} input impedance of the structure becomes:

$$Z'_{eq} = \frac{C + C_{pv}}{CC_{pv}} \frac{1}{\beta} \frac{\alpha}{s} + \frac{C + C_{pv}}{CC_{pv}} \frac{1}{\beta} \frac{\beta - \alpha}{s + \beta} \tag{44}$$

or:

$$Z'_{eq} = \frac{V_i}{I_c} = \frac{1}{sC_{ssv}} + \frac{\frac{1}{C_{ppv}}}{s + \frac{1}{C_{ppv}R_{ppv}}} \tag{45}$$

The last relationship shows that Z_{eq} corresponds to the circuit in Fig. 10, the parameters of which being given by:

$$C_{ssv} = \Big(1 + \frac{g_{m1}}{g_{m2} + g_o}\Big)C = (1 + K_v)C \tag{46}$$

$$C_{ppv} = \frac{1}{1 + \frac{g_{m1}}{g_{m1}+g_{m2}+g_o}\frac{C_{pv}}{C}} C_{pv} = \frac{1}{1 + \frac{K_v}{K_v+1}\frac{C_{pv}}{C}} C_{pv} \tag{47}$$

$$R_{ppv} = \frac{1}{g_{m1} + g_{m2} + g_o}\Big(1 + \frac{K_v}{K_v + 1}\frac{C_{pv}}{C}\Big) \tag{48}$$

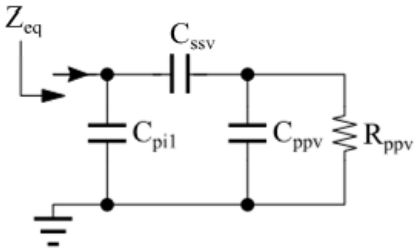

Fig. 10. Input impedance equivalent model for the voltage mode capacitance multiplier.

In the previous relations $K_v = g_{m1}/(g_{m2}+g_o)$ is the multiplication factor adjustable by g_{m1} and g_{m2}. In ideal conditions, with $C_{pi1,2} = C_{po1,2} = 0$ and $g_{o1,2} = 0$, the equivalent circuit is reduced to the one in Fig. 4 as emphasized by the relationships (49) and (50):

$$C_{ssv} = C_{eq} = C\Big(1 + \frac{g_{m1}}{g_{m2}}\Big) \tag{49}$$

$$R_{ppv} = R_{eq} = \frac{1}{g_{m2} + g_{m1}} \tag{50}$$

By comparing the equivalent models of the two possible implementations of the G_m based capacitance multiplier, we can see that, since the voltage mode structure equivalent model does not exhibit an equivalent parallel input resistance, it is expected for this structure to have a strong capacitive behaviour even at low frequency, while for the current mode structure the low frequency dominant element is g_{o1}.

Also, by comparing the expressions of the multiplication factor for the two implementations, it can be noticed that the current mode implementation allows obtaining slightly higher equivalent capacitances due to the fact that the denominator is smaller $(g_{m2}+g_{o2})$ as compared to the voltage mode one $(g_{m2} + g_{o1} + g_{o2})$.

Another expected consequence when using the voltage mode multiplier is a poorer dynamic range, *i.e.* there is a trade-off between frequency behaviour and dynamic range.

6. Simulation results

The two circuit solutions have been simulated using the AMS 0.18um CMOS PDK.

In order to evaluate the behaviour of the voltage mode multiplier and to make a comparison against the current mode one, an elementary transconductor implementation has been used, as illustrated in Fig. 11. The common mode feedback circuit, required for the g_{m1} transconductor, is not shown.

Source degeneration has been used to achieve the transconductor's adjustability. The degeneration resistor is implemented using a linear region biased transistor, as proposed in [5]. An additional parallel connected resistance has been used in order to improve the linearity of the first stage, voltage to current converter, of the transconductance amplifier. Source degeneration has been used to achieve the transconductor's adjustability. The degeneration resistor is implemented using a linear region biased transistor, as proposed in [5]. An additional parallel connected resistance has been used in order to improve the linearity of the first stage, voltage to current converter, of the transconductance amplifier.

For each transconductance amplifier in Fig. 2b/2c, the transconductance is controlled by the I_{TUNE} current. The control has been done by keeping constant the sum of the tuning currents. When the g_{m1} transconductor tuning current is increased, the corresponding tuning current of the g_{m2} transconductor is decreased such that the sum of the two tuning currents is 25uA.

The simulation results illustrated in Fig. 13 agree with the expected behaviour theoretically derived. The voltage mode multiplier tuning range is $1pF \ldots 28pF$ by using a $1pF$ base capacitor, value slightly lower than that obtained for the current mode multiplier ($\sim 29pF$), as explained previously. The magnitude and phase of the input impedance for the voltage mode multiplier compared to the current mode one are illustrated in Fig. 12. It can be observed that the Miller structure presents a capacitive behavior for a larger frequency domain compared to the current-mode multiplier performance.

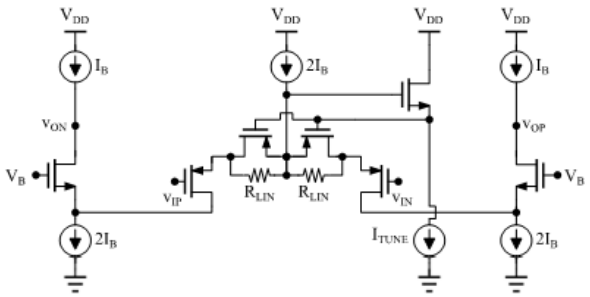

Fig. 11. Implementation of the tunable transconductor.

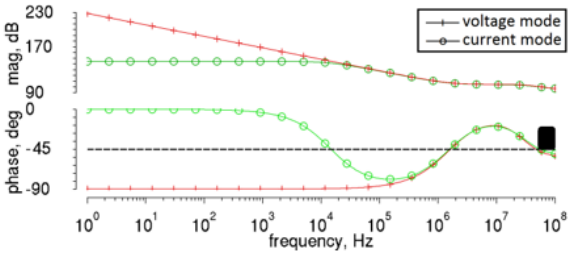

Fig. 12. Magnitude an phase of the input impedance for different values of tune current.

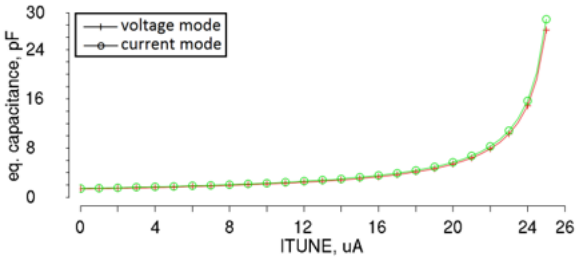

Fig. 13. Equivalent input capacitance versus tune current.

7. Physical implementation using discrete Gm ICs

The two G_m based capacitance multiplier architectures have been implemented using the LM13700 Dual Operational Transconductance Amplifier IC (without connecting the Darlington output stage). The purpose of the physical implementation has been to indirectly characterize the performances of the current mode and voltage mode capacitance multipliers with emphasis on the low frequency behavior.

As an application, a first order LPF was implemented on two printed circuit boards (PCBs), one utilizing the current mode capacitance multiplier and another one utilizing the voltage mode capacitance multiplier, as depicted (simplified) in Fig. 14 and Fig. 15. By measuring the frequency response of the two LPFs, one can indirectly measure the value of the multiplied capacitance and its parallel resistance. For both architectures, the tunability of the multiplication factor was implemented using the R_P potentiometer. The transconductance of amplifiers is determined by the value of the supply voltage V_{CC} and the values of R_P, R_{B1} and R_{B2}.

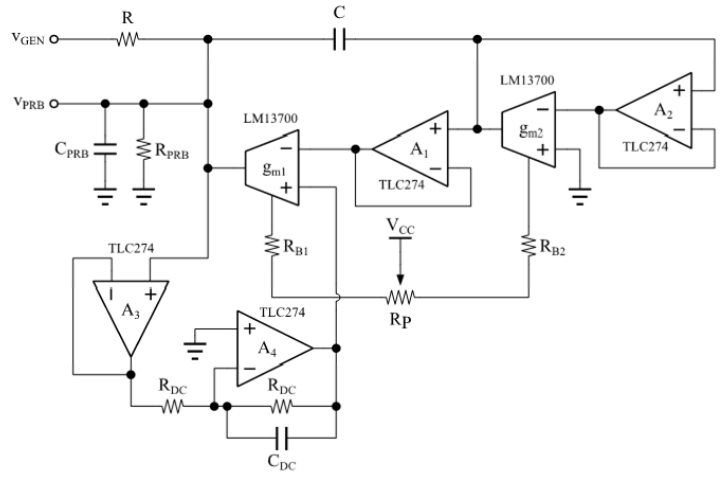

Fig. 14. LPF that uses the current mode capacitance multiplier implemented using LM13700.

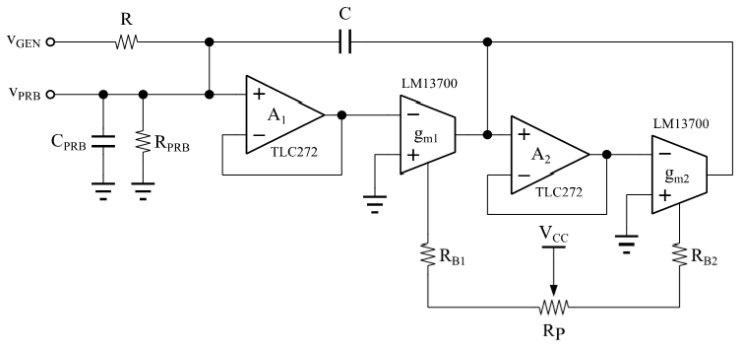

Fig. 15. LPF that uses the voltage mode capacitance multiplier implemented using LM13700.

Given the poor input impedance of the LM13700 (BJT implemented input stage), the TLC27x double/quad operational amplifiers IC has been used to implement input buffers for each transconductor amplifier. For the case of the LPF implemented with the current mode capacitance multiplier (Fig. 14), a supplementary feedback loop has been used to define the DC voltage of the high-impedance node between R and C. The feedback loop is comprised of the A_3 voltage buffer and the DC voltage level extractor implemented with the very low-pass filter built around A_4.

The R_P potentiometer is implemented using a multiturn potentiometer exhibiting about 26 turns (in practice 24 to 27 turns), such that the resistances of the two arms of the potentiometer can be expressed as:

$$R_P = R_{P1} + R_{P2} = R_{P1} + kR_{STEP} \tag{51}$$

where R_{STEP} is the resistance variation of one potentiometer step. The LM13700 transconductance is proportional to the bias current, therefore one can write:

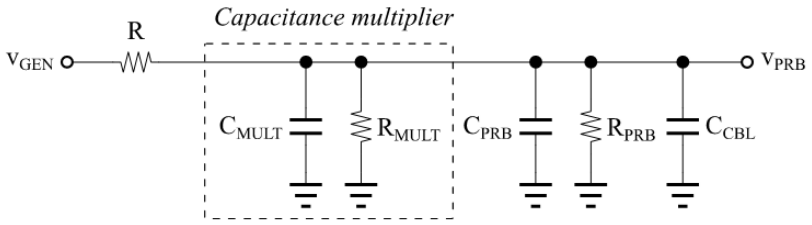

Fig. 16. Equivalent circuit of the LPF with any of the capacitance multipliers (either current or voltage mode).

$$g_{m1} \approx \frac{const.}{R_{B1} + R_{P1}} = \frac{const.}{R_{B1} + R_P - kR_{STEP}} \tag{52}$$

$$g_{m2} \approx \frac{const.}{R_{B2} + R_{P2}} = \frac{const.}{R_{B2} + kR_{STEP}} \tag{53}$$

The capacitance realized by the capacitance multiplier, C_{MULT} can be written as:

$$C_{MULT} = \left(1 + \frac{g_{m1}}{g_{m2}}\right) C \approx \left(1 + \frac{R_{B2} + kR_{STEP}}{R_{B1} + R_P - kR_{STEP}}\right) C \tag{54}$$

The cutoff frequency of the circuit in Fig. 16 is given by

$$f_c = \frac{1}{2\pi(R||R_{MULT}||R_{PRB})(C_{MULT} + C_{PRB} + C_{CBL})} \tag{55}$$

where R_{MULT} is the equivalent parallel resistance of the capacitance multiplier (denoted as g_{o1} in Fig. 7), R_{PRB} is the input resistance of the oscilloscope, C_{PRB} is the input capacitance of the oscilloscope and C_{CBL} is the parallel capacitance of the cable used to connect the output of the LPF to the oscilloscope. The DC gain of the LPF is given by

$$a_0 = \frac{R_{MULT}||R_{PRB}}{R + R_{MULT}||R_{PRB}} \tag{56}$$

Equations (54)-(55) hints to the methodology used in this work to determine R_{MULT} and C_{MULT} indirectly: by measuring the DC gain of the LPF one can determine $R_{MULT}||R_{PRB}$, and by measuring the cutoff frequency of the LPF one can determine $C_{MULT}+C_{PRB}+C_{CBL}$. Considering $R_{PRB}, C_{PRB}, C_{CBL}$ to be known, one can determine R_{MULT} and C_{MULT}.

8. Measurement results

The measurements were performed using the Digilent Analog Discovery 2 data acquisition module. The position of the R_P multiturn potentiometer cursor has been varied manually in complete turns (such that the potentiometer arms resistance has been varied by R_{STEP} for each measurement). For each potentiometer turn the frequency response of the LPF has been measured by applying a sinusoidal 100mV voltage at the input of the LPF (v_{GEN}) and measuring the response of the LPF at the output (v_{PRB}) for a range of frequencies (from 10Hz to 100kHz, 201 points, 50 points per decade).

Fig. 17/18 show the measured frequency response of the LPF that uses the current/voltage mode capacitance multiplier. It can be observed that the low frequency gain of the LPF using the voltage mode capacitance multiplier is higher (-6.03dB vs -6.05dB) and does not vary (in contrast to the low frequency gain of the LPF using the current mode capacitance multiplier, which varies with the variation of the multiplication factor).

Fig. 19/20 illustrates the tuning range of the equivalent input capacitance of the current/voltage mode capacitance multiplier: data points along with the curve described by the following equation:

$$C_m = C_{MULT} + C_x = \left(1 + \frac{R_{B2} + kR_{STEP}}{R_{B1} + R_P - kR_{STEP}}\right) C + C_x \tag{57}$$

where C_m is the capacitance used for the curve fitting, C_{MULT} is the capacitance of the multiplier and C_x totalizes the parasitic capacitances (osciloscope input capacitance C_{PRB}, cable capacitance C_{CBL}, etc).

The cutoff frequency of the LPF that uses the current/voltage mode capacitance multiplier is plotted in Fig. 21/22 while the equivalent parallel input resistance of the current/voltage mode capacitance multiplier is depicted in Fig. 23/24.

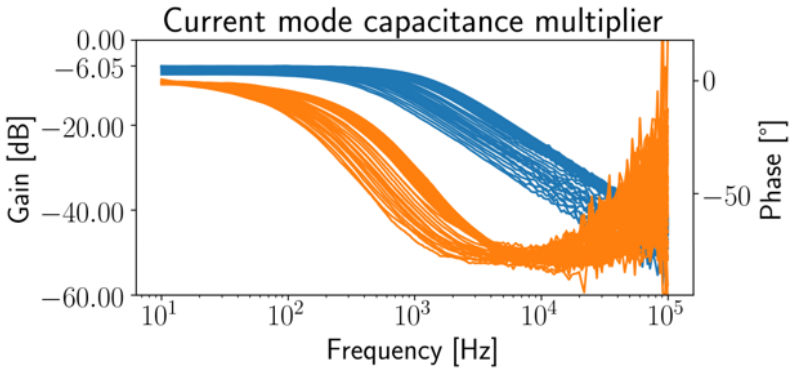

Fig. 17. Frequency response of the LPF that uses the current mode capacitance multiplier

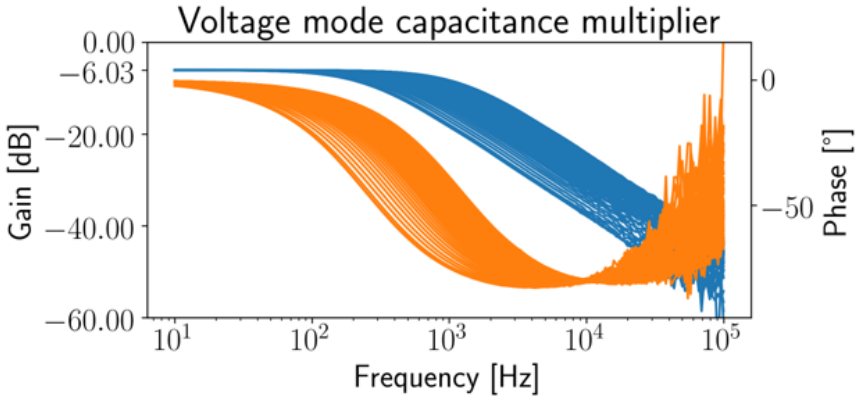

Fig. 18. Frequency response of the LPF that uses the voltage mode capacitance multiplier.

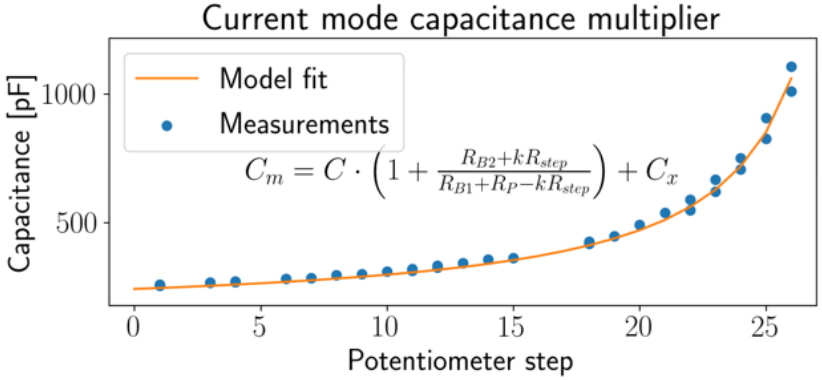

Fig. 19. Equivalent input capacitance of the current mode capacitance multiplier.

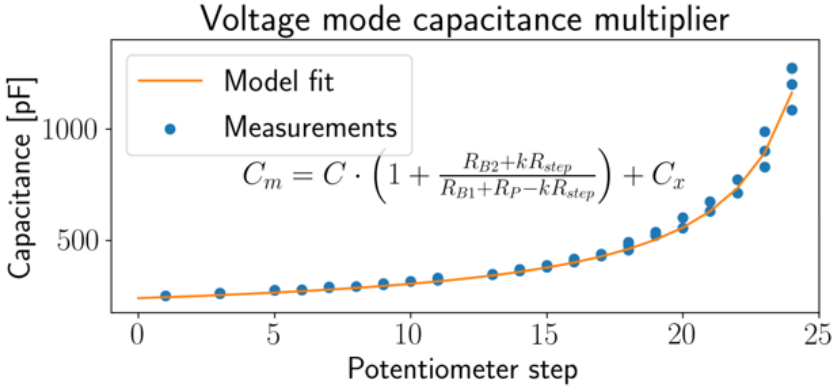

Fig. 20. Equivalent input capacitance of the voltage mode capacitance multiplier.

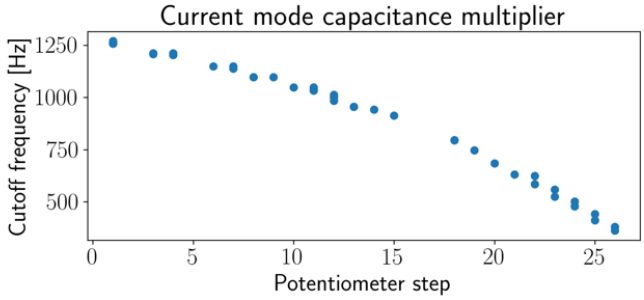

Fig. 21. Cutoff frequency of the LPF that uses the current mode capacitance multiplier.

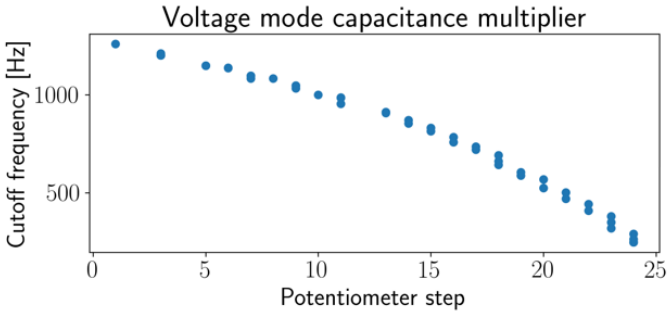

Fig. 22. Cutoff frequency of the LPF that uses the voltage mode capacitance multiplier.

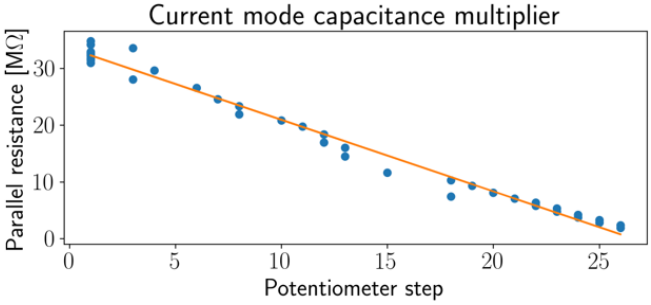

Fig. 23. Equivalent parallel input resistance of the current mode capacitance multiplier.

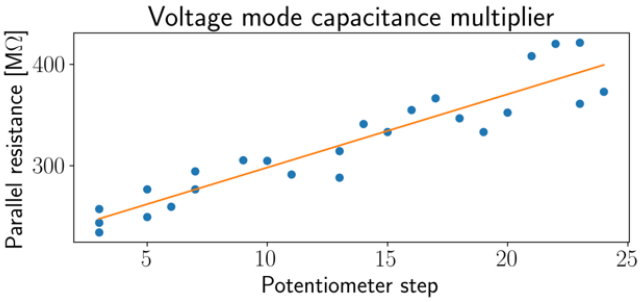

Fig. 24. Equivalent parallel input resistance of the voltage mode capacitance multiplier.

The measurement results confirm that the voltage mode multiplier has a capacitive behavior for much lower frequencies and a much higher input resistance than in the case of the current mode multiplier (the smallest input resistance of the voltage mode multiplier is about 10 times larger than the largest input resistance of the current mode multiplier). Fig. 23 and 24 contain a smaller number of measurements to improve the visualization of the results (for comparison purposes the higher values of the input resistance have been selected for the current mode capacitance multiplier while the lower values of the input resistance have been selected for the voltage mode capacitance multiplier).

9. Conclusion

In this paper a comparison between the G_m based implementations of the capacitance multipliers with voltage mode and current mode respectively has been performed. The two G_m based current mode capacitance multiplier architectures have been studied by considering the input impedance, the frequency behaviour and the tunability range.

A first order LPF has been implemented as application using discrete Gm ICs for both architectures.

There is a good agreement between the theoretical expectations and the simulation/measurement results.

Compared to the current mode implementation, the voltage mode architecture exhibits an improved low frequency behaviour due to its almost pure capacitive input impedance, while exhibiting practically similar adjustability performances. Due to limited voltage swing, the voltage mode can be used in target applications where frequency compensation is built around nodes with reduced swing.

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