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Design of Over-Temperature Protection for Switched-Capacitor DC-DC Converter Based on Electro-Thermal Simulations

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Abstract. This paper presents an over-temperature protection (OTP) circuit for a DC-DC converter based on switching capacitors (SC DC-DC). A two-steps design methodology was employed: a first-pass circuit was obtained by using standard, electrical-only simulations; next, electro-thermal simulations were employed to ascertain the best location of the thermal sensor and the resulting thermal coupling, thus allowing for the fine-tuning of the final circuit. The die temperature distribution was analyzed for two critical operational scenarios in order to identify the worst case and to provide design data for implementing a robust and precise OTP. The key electrical and electro-thermal simulation results are presented in some detail. Finally, results of measurement performed on the actual silicon are presented, to validate the design.

Key-words: Over-temperature protection; switched-capacitor DC-DC converter; controlled charging current, thermal shutdown; electro-thermal simulations.

1. Introduction

DC-DC converters based on switching capacitors (SC DC-DC) have become real challengers to inductor-based converters for low- to medium- power automotive applications [1]. External inductors are not only expensive but also bulky and susceptible to mechanical vibrations.

Over-temperature protection (OTP) is a basic feature for linear voltage regulators, essential for avoiding physical destruction in fault conditions such as output shorted to ground [2]. Even though the SC DC-DC operates at high efficiency an accurate OTP is necessary to protect the converter against thermal runaway phenomena that can appear in certain situations [3].

Section 2 presents the core of the SC DC-DC converter considered in this paper, highlighting the operational conditions that can result in substantial levels of dissipated power, as well as the main design options for the circuit-level implementation of an OTP circuit for this converter.

A design example is presented in some detail in Section 3. It proposes a two-steps design methodology: a first version of the OTP circuit is designed using standard, electrical-only simulations; next, electro-thermal simulations are employed to choose the best location of the thermal sensor and to derive the resulting thermal coupling between the temperature sensor and the hot-spots within the power switch of the converter, thus providing essential data for fine-tuning the circuit. These design steps are illustrated by key electrical and electro-thermal simulation results. Results of measurements performed on the silicon implementation of the designed SC DC-DC converter are also shown, in order to validate the design.

The main points are summarized in the final Section, which also presents the main conclusions one can draw from this work.

2. OTP for a SC DC-DC Converter with Controlled Charging Current

A. Core Schematic and the Case for OTP

The core of a SC DC-DC converter is the switched capacitor array which consists of MOS switches and "flying" capacitors (C_{FLY}) used for storing and transferring energy. Of the many possible topologies, the 2:1 (step-down) or 1:2 (step-up) configuration was chosen for the discussion here, as they are among the most used SC DC-DC converter topologies. In general, they provide good efficiency and require a relatively small die area, due to their employing only one C_{FLY} [4-10]. Moreover, we focused on the implementation shown in Fig. 1, a one-C_{FLY} SC DC-DC with controlled charging current.

The circuit converts the input voltage, V_{IN}, into a regulated output voltage, V_{OUT} within two phases: C_{FLY} is charged from the input in the first phase ($\Phi 1$) and discharged on the load in the second phase ($\Phi 2$). This is achieved by turning ON switches S2 and S4 during phase $\Phi 1$ and switches S1, S3 and S5 during phase $\Phi 2$. The output voltage level is set and maintained by a feedback loop that controls the amount of charge transferred from the input to the output. The transferred charge is sourced by a power current mirror (PCM – transistors M2 and M3); the amount of charge transferred is set by the differential error amplifier (EA) that drives transistor M1 proportionally to the difference between the voltages applied to its inputs: the reference V_{REF} and a fraction of the output voltage brought to the inverting EA input by the resistive divider R_1, R_2 (V_{FB}). The two equivalent circuits corresponding to each phase of operation are presented in Fig.2.

In normal operation conditions the power dissipated on switches S1 - S4 is not large enough to cause their overheating. But in certain operational scenarios large voltage drops can appear across the power transistor M3 within the PCM which can result in substantial levels of dissipated power. Here are two such critical scenarios:

- Normal start-up but a large input voltage is applied. The PCM will source the maximum possible current in the first phase (Φ_1) because the inputs of the EA are totally unbalanced, as V_{FB}=0. Until the steady state is reached (that is, until $V_{FB} = V_{REF}$) a large amount of power is dissipated by the PCM in each phase Φ_1.

- Start-up in shorted-output fault condition (the output shorted to ground). In this scenario the inputs of the EA remain unbalanced all the time and the PCM will try to source the maximum possible current in each phase Φ_1.

The designer should ensure that in all valid operational scenarios the maximum die temperature within the converter – called here $T_{HOTSPOT}$ - remains below a safe value, defined by application and technology limits.

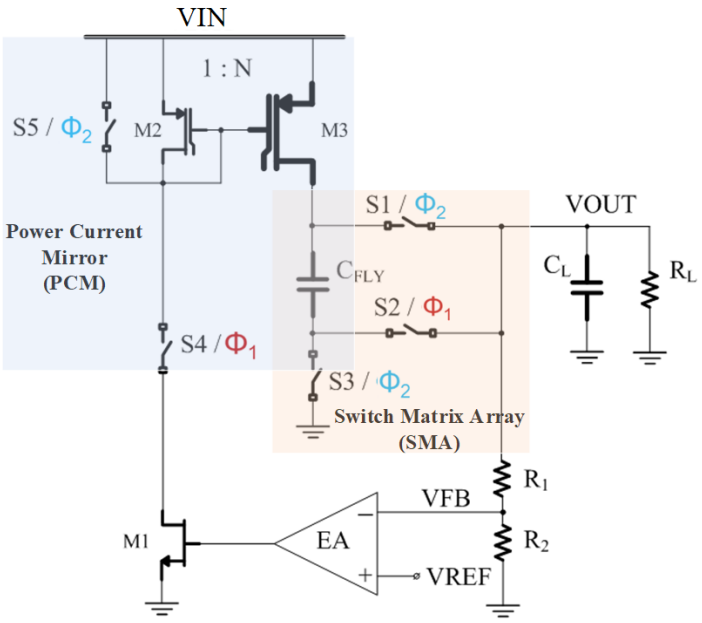

Fig. 1. Core schematic of a SC DC-DC converter with controlled charging current.

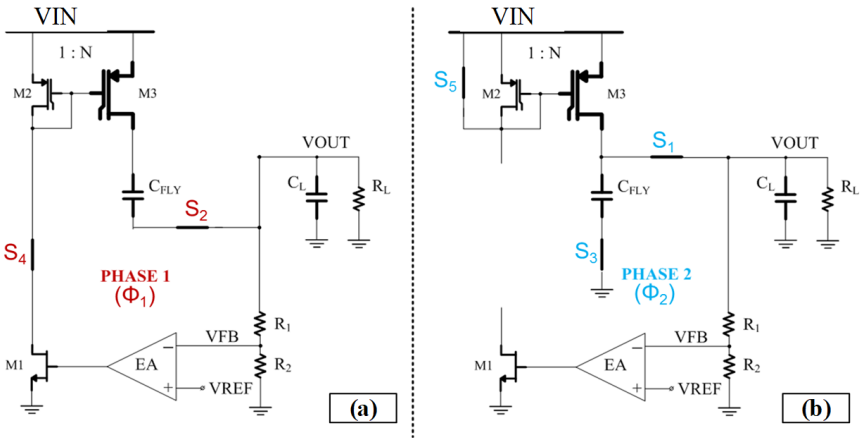

Fig. 2. Equivalent circuits corresponding to each phase of operation of the SC DC-DC converter with controlled charging current ((a) - Phase 1 and (b) - Phase 2).

B. Design Options for Circuit Implementation of OTP

Fig. 3 presents a typical circuit implementation of the OTP, usually employed for LDOs [11] but which can be adapted for SC DC-DC converters, as well.

The voltage produced by a temperature sensor, OTP_{SENSOR} – here the base-emitter voltage of a BJT, V_{EB} – is applied to the inverting input of a voltage comparator with hysteresis, implemented by the operation amplifier, the gain stage based on transistor T_1, and the Schmitt Trigger that selects the reference voltage applied to the non-inverting input, V_{REF1} or V_{REF2}. When the temperature of the OTP_{SENSOR} goes above the activation temperature of the OTP circuit - called here T_{HIGH} -, the output OTP_{OUT} will go to logic "1"; when the temperature goes below the de-activation temperature – called here T_{LOW} -, the OTP_{OUT} will trip to logic "0".

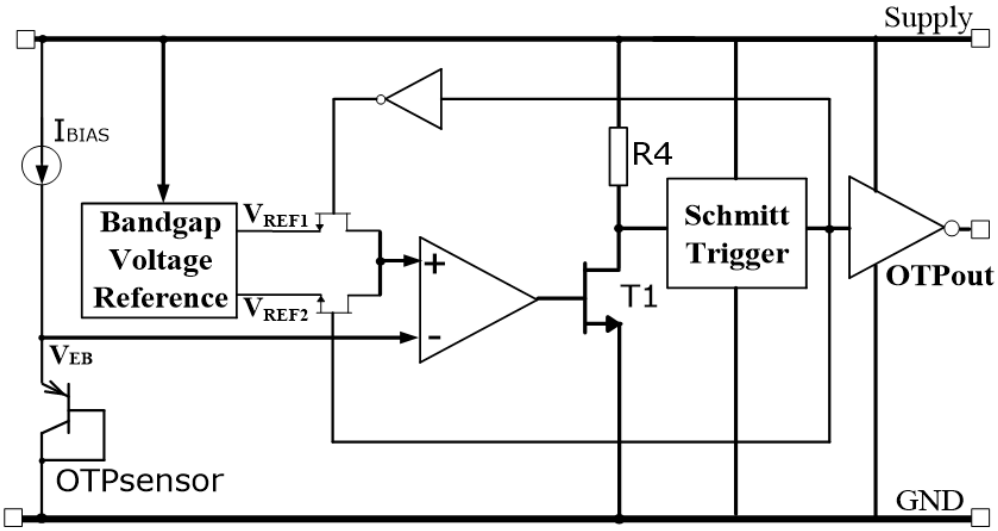

Fig. 3. Schematic of the proposed OTP.

For the SC DC-DC topology shown in Fig. 1 the OTP_{OUT} signal can be used to implement the OTP in three different ways, illustrated in Fig. 4:

- Method 1: The OTP_{OUT} signal can be used as a control signal for the PCM. When an OTP event occurs the OTP_{OUT} goes high, and a logic circuit can turn ON the switch S_5 and turn OFF the switch S_4.
- Method 2: The OTP_{OUT} signal is used as an additional input to the Digital Control Block (DCB) of the converter so that when OTP_{OUT} goes high the DCB will activate phase Φ_2 and keep the converter in that state until the OTP_{OUT} signal goes low, that is, until the temperature of the OTP_{SENSOR} drops below T_{LOW}.
- Method 3: The OTP_{OUT} signal can be used as an additional enabling condition for the oscillator that generates the Φ_1 and Φ_2 clocks: the oscillator is turned off as long as OTP_{OUT} stays high.

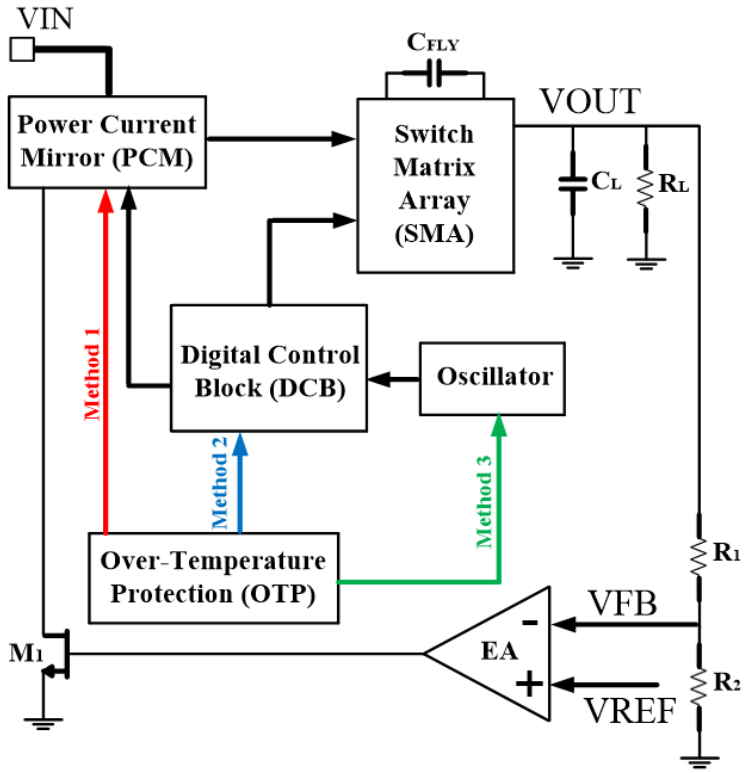

Fig. 4. Simplified block diagram of a SC DC-DC Converter with Over-Temperature Protection (OTP).

3. Design Example

A. Requirements for the OTP circuit

The maximum temperature of the SC DC-DC converter can be maintained bellow a safe threshold only by optimizing the power distribution within the PCM and by minimizing the temperature difference between the hot-spot and the OTP_{SENSOR}.

The following design requirements for the OTP circuit were set:

- the value of the activation temperature: T_{HIGH}=175°C,
- the value of the de-activation temperature (and implicitly the hysteresis width): T_{LOW}=160°C - large enough to avoid thermal toggling around the activation threshold.

The electro-thermal phenomena and the requirements mentioned before will impact directly the temperature of the hot-spot which indicates the necessity of a systematic approach.

B. Design Steps

Fig. 5 presents the floorplan of a SC DC-DC converter we designed for a specific application, based on the schematic shown in Fig. 1. A version of the OTP circuit shown in Fig. 3 was also

integrated. Method 2 described above was used to implement the OTP: the SC DC-DC converter was kept in phase Φ_2 as long as OTP_{OUT} had a logic "1" value.

The methodology used to design the OTP circuit relies on two important steps which correspond to the simulation type performed: electrical-only simulations and electro-thermal simulations.

Step 1 = the circuit was sized by using electrical-only simulations, aiming for the desired T_{HIGH} and T_{LOW} ; Quite often OTP circuits are designed based on electrical-only simulations. But these simulations assume that the die temperature is constant across the entire converter, which is obviously not the case in a real-life integrated circuit (IC); therefore, the designed/simulated OTP activation and de-activation temperatures can be quite far from their actual, measured values.

– Fig. 6 presents results from a temperature sweep simulation; one can derive the activation (T_{HIGH}) and the de-activation temperature (T_{LOW}) for the OTP. The value of T_{HIGH} has a direct impact on the maximum temperature within the entire converter therefore its deviation due the process variation needs to be considered. Fig. 7 presents Monte Carlo simulations results for T_{HIGH} value computed for 500 runs.

– Fig. 8 presents the output of the SC DC-DC converter yielded by a transient simulation that also involved changing the die temperature. Until t=165us the die temperature was kept constant, T=165°C; afterwards the temperature was increased by 1°C/us. Thus, at around t=175us the OTP activation temperature, T_{HIGH}, was reached, OTP_{OUT} went high and the SC DC-DC converter was held in phase Φ_2 (Fig. 2 (b)). Therefore, the output voltage dropped to zero as C_{FLY} discharged through the load.

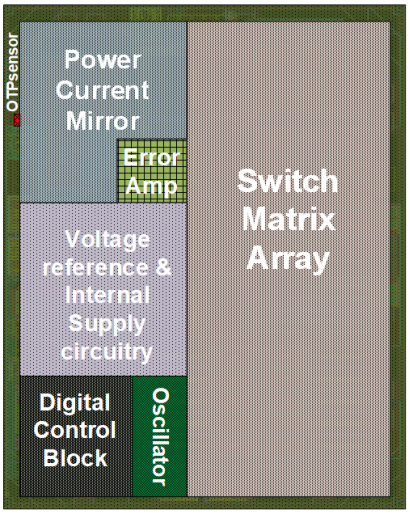

Fig. 5. Floorplan of a SC DC-DC converter with controlled charging current and OTP designed based on Figs. 1-3.

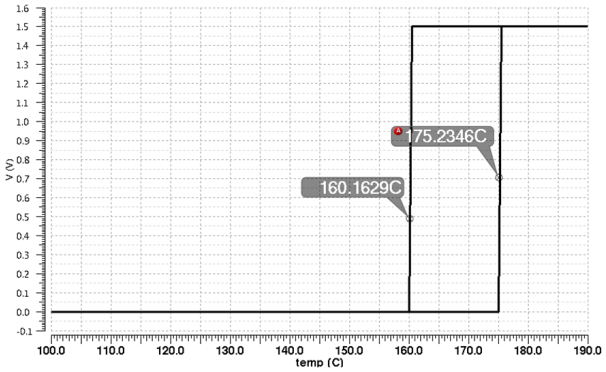

Fig. 6. OTP_{OUT} variation when die temperature is sweep from 100°C to 190°C (output goes from low to high at 175.23°C), then from 190°C to 100°C (output goes from high to low at 160.16°C).

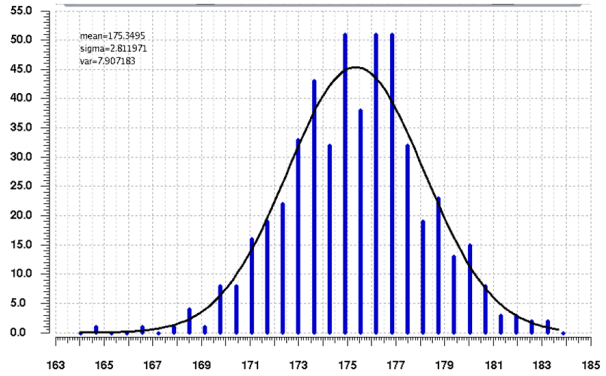

Fig. 7. Monte Carlo (mismatch and process variation) simulation results for T_{HIGH}.

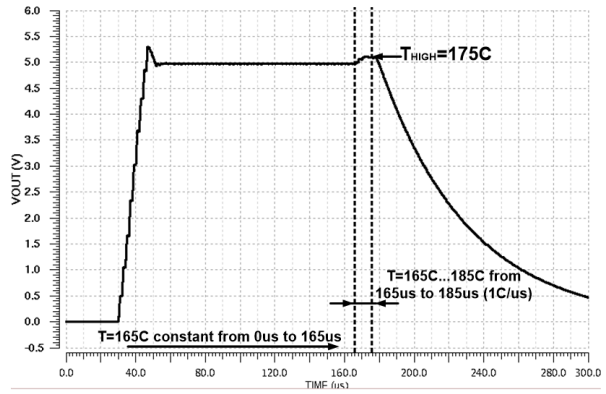

Fig. 8. The SC DC-DC output voltage when the die temperature was increased by 1°C/us, starting at t=165us.

Step 2 = finely adjust the circuit based on electro-thermal simulations run as described in [12], but considering the critical scenarios presented in Section 2.A. The main results are: the maximum temperature that can appear within the IC ($T_{HOTSPOT}$) and the hot-spot location. These data are necessary for deciding the OTP_{SENSOR} location and for calculating the resulting thermal coupling:

$$DeltaT[^{\circ}C] = T_{HOTSPOT} - T_{OTP_{SENSOR}} \quad (1)$$

The electro-thermal simulations consider the IC layout, the physical description of the package, the ambient temperature (T_{START}) and the power dissipated by the PCM yielded by electrical-only simulations (Fig. 9).

Table 1 summarizes results of tests run for the two critical scenarios with T_{START} set to -40°C or 150°C. The worst case DeltaT value was obtained for the "start-up in fault condition" test, with T_{START}=150°C: DeltaT= 65°C. Fig. 10 presents electro-thermal simulation results for this case: it shows the variation over time of temperatures $T_{HOTSPOT}$ (red trace) and $T_{OTP_{SENSOR}}$ (black trace). Note that the PCM temperature, from where $T_{HOTSPOT}$ is extracted, varies: in Φ_1 the temperature increases as power is dissipated by the PCM) while in Φ_2 the temperature decreases because the PCM dissipates no power. Overall the PCM temperature increases until the temperature of the OTP_{SENSOR} reaches the T_{HIGH} threshold. The thermal-map is also presented in Fig. 10 (right-hand side).

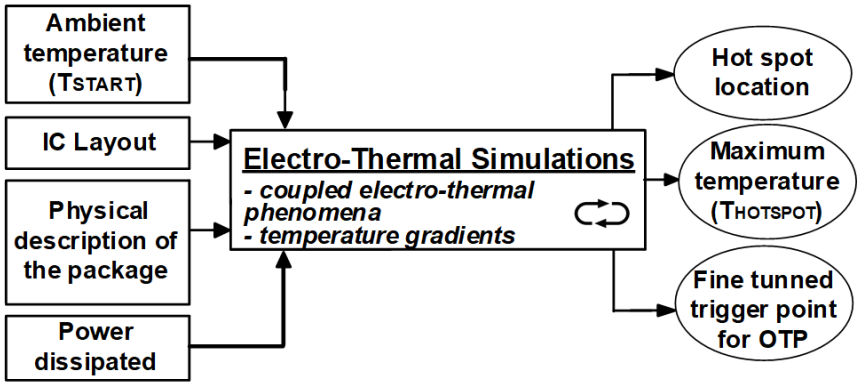

Fig. 9. Electro-thermal simulations: inputs and outputs.

Table 1. DeltaT[°C] yielded by electro-thermal sims

DeltaT [°C]		
Test scenario (Section 2.A)	T_{START} =–40°C	T_{START} =–150°C
Normal Start-up	8.5°C	16.5°C
Start-up in fault condition	52°C	65°C

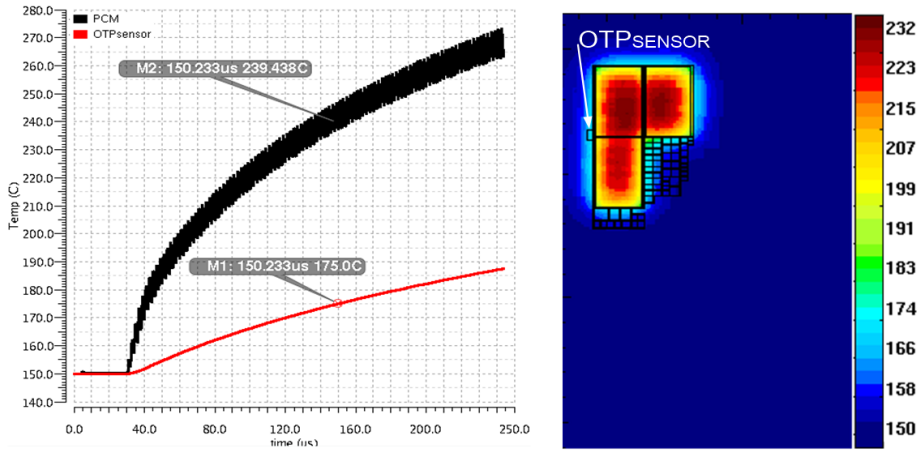

Fig. 10. Left: Temperature variation over time for the OTP_{SENSOR} (red) and for the hot-spot within the PCM (black). Right: The corresponding temperature map of the SC DC-DC converter at time=150us, when the OTP is activated.

Temperature distribution maps for three possible locations of the OTP sensor are presented in Fig. 11: (a) the OTP_{SENSOR} is placed center-right towards the PCM (OTP_{SENSOR}_right), (b) the OTP_{SENSOR} is placed on the left side of the PCM (OTP_{SENSOR}_left) and (c) the OTP_{SENSOR} is placed above the PCM (OTP_{SENSOR}_top). The temperature maps are obtained after applying the same scenarios used for Fig. 10 except the fact that in this case it was used the mean power to reduce the simulation time (the error regarding the DeltaT value is less than 10°C). The temperature maps are evaluated at the OTP event – when the temperature on the OTP_{SENSOR} reached the T_{HIGH} value. The arrangement with more uniform temperature distribution is the one showed in Fig. 11 (a) (it is visible that the maximum temperature in this case is below 205°C) followed by the configuration with the OTP_{SENSOR} placed on the left side of the PCM ($T_{HOTSPOT} < 228$°C).

Fig. 11 (d) shows the temperature variation of the hottest (hotspot) unit of the PCM as well as for the three OTP_{SENSOR} positions discussed before. It can be seen that the best DeltaT [°C] is obtained when the OTP_{SENSOR} is placed on the right side (DeltaT [°C] = 33°C) while the worst thermal coupling is obtained when the OTP_{SENSOR} is placed above the PCM (DeltaT [°C] = 78°C). The second-best option (DeltaT [°C] = 58°C) was chosen for out implementation because the layout implementation for the first one was quite difficult and the difference between the first two best options is not large enough to affect the electro-thermal reliability of the converter.

In general, results of electro-thermal co-simulation are difficult to validate through direct measurements. We devised the following test scenario: the start up in normal operation presented in section 2.A. but with a different value for the output current (in order to maintain the PCM in the safe operating area and to avoid the influence of the current limit circuitry); the main simulation – and measurement – result is the time it takes for the OTP to be activated. Another issue is the amount of time and resources required by electro-thermal co-simulations, especially for switching converters.

A simple, yet effective solution to this issue is based on the fact that it is sufficient to simulate only the Phase 1 (Fig. 2 (a)) because only in that phase power is dissipated on the PCM; in this case, the load current is approximately equal to the mean value for the two phases. This simplified, continuous-time circuit emulates with a good approximation the behavior of the actual, SC

DC-DC converter, with respect to electro-thermal effects.

The designer should take into consideration the $\pm 10°C$ variation of the maximum temperature as seen in Fig. 10 given by the two-phases operation. The C_{FLY} capacitor was replaced in these simulations by a simple DC voltage source, with the value set to the normal voltage developed across C_{FLY}. The inputs for the electro-thermal co-simulation are the same as those presented in Fig. 9, with the circuit netlist modified as to fit the configuration described above. A more detailed description of such electro-thermal co-simulations is presented in [13].

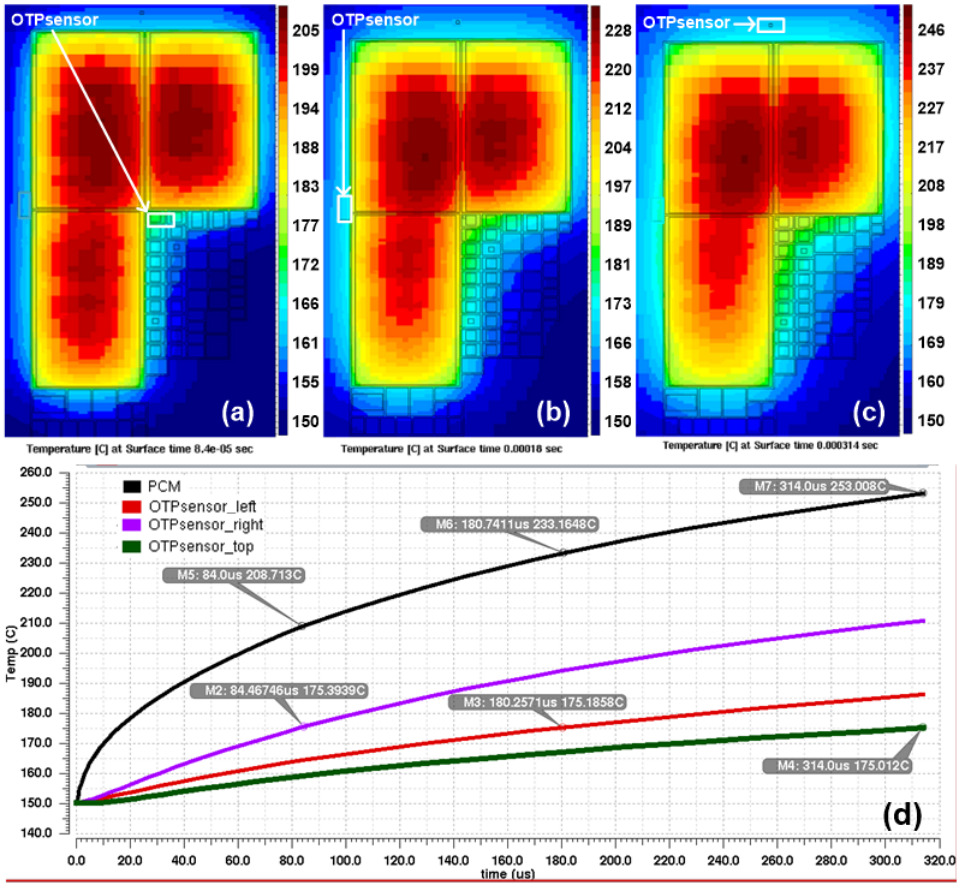

Fig. 11. Temperature maps for the three different positions of the OTP_{SENSOR}: (a) center-right position towards PCM, (b) left side of the PCM and (c) the OTP_{SENSOR} placed above the PCM. (d) The corresponding temperature variation over time for the three positions of the OTP_{SENSOR} and for the hot-spot within the PCM.

The electro-thermal co-simulation results are presented in Fig. 12. The dynamic behavior of the SC DC-DC converter at OTP event can be seen by monitoring the output voltage (VOUT) corelated with the temperature values on the OTP_{SENSOR} and on the PCM (where the hot-spot is located). The DeltaT [°C] can be extracted before the OTP event and proves that $T_{HOTSPOT}$ is at a safe level.

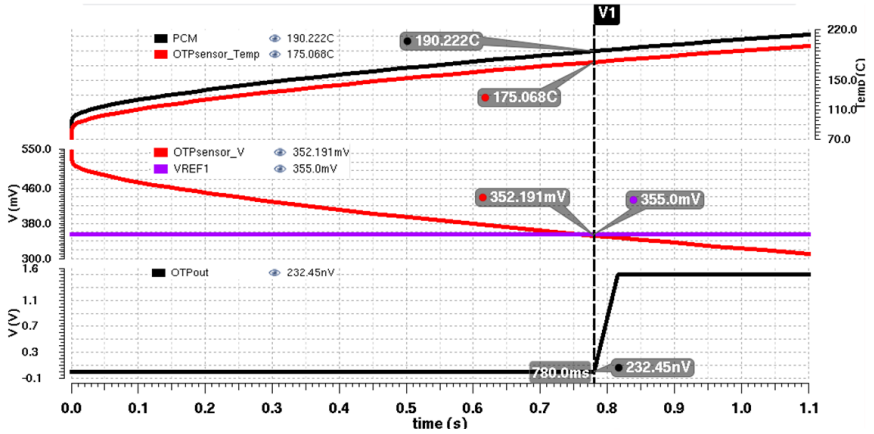

Fig. 12. Temperature variation over time for the OTP_{SENSOR} (top plot - red) and for the hot-spot within the PCM (top plot - black) – for the specific test scenario. Voltage variation over time for the OTP_{SENSOR} (middle plot - red), for the reference used as threshold (middle plot - purple) and for the OTP_{OUT} (bottom plot - black) – the output of the OTP circuity.

C. Measurements Results

The SC DC-DC converter described above was implemented in a standard CMOS technology. The OTP thresholds were measured using a testbench similar to the one used for the simulation results obtained in Fig. 6. The ambient temperature was set by a system based on controlled air flow and was gradually increased in 1°C steps, while monitoring the output voltage, VOUT. The load current was set to a very small value, so that the effect of the power dissipation on the SC DC-DC converter to be minimal. When the OTP event occurs the output voltage drops to zero, and the OTP activation temperature, T_{HIGH} , is simply the temperature set by the air-flow system at that moment. Then, the OTP de-activation temperature, T_{LOW} , can be measured by decreasing progressively the temperature of the SC DC-DC converter until the output voltage returned to its nominal value. The measurements were performed on three samples as shown in Fig. 13; the resulting values for T_{HIGH} and T_{LOW} are:

- S1: T_{HIGH} = 173°C and T_{LOW} = 158°C (blue trace);
- S2: T_{HIGH} = 175°C and T_{LOW} = 160°C (green trace);
- S2: T_{HIGH} = 176°C and T_{LOW} = 161°C (black trace);

The simulation scenario considered in the previous Section, that yielded the results shown in Fig. 12 was reproduced on the laboratory testbench; the resulting measurements are shown in Fig. 14. The dynamic behavior of VOUT is presented with highlights on three important events: Z1 – the moment the first OTP event occurs (t_{2OTP}=785ms approximately), Z2 – the moment when the thermal stability of the converter for this test scenarios is reached and Z3 – the detailed behavior of the VOUT when an OTP event is reached (the counterpart of Fig. 8 – the discharge time of the VOUT is approximately the same around 50us). As can be seen there is a good correlation between the t_{2OTP} measured and simulated, 785ms and 780ms respectively which validates the design methodology proposed.

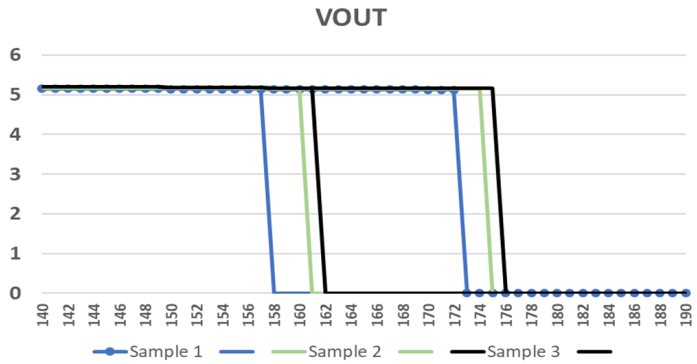

Fig. 13. T_{HIGH} and T_{LOW} values extracted from measurements on 3 samples.

Moreover, it offers to the designers the control regarding the maximum temperature on the entire converter by having a good correlation between the measurement and the electro-thermal simulations. The good correlation between Z3 and Fig. 8 shows that the behavior of VOUT is as expected: after the OTP event, the converter operates in phase Φ_2 – Fig. 2(b) (Method 2) and in this phase the two capacitors are placed in parallel (C_{FLY} and C_L) and are discharged through the resistive load (R_L). Note that the measurements were not performed in a low EMI environment, hence the large ripple on the output voltage; however, this ripple has no significant effect on the t_{2OTP} value. By comparing Fig. 12 and Fig. 14 one can notice the fairly good correspondence between electro-thermal simulations and measurements performed on the integrated SC DC-DC converter.

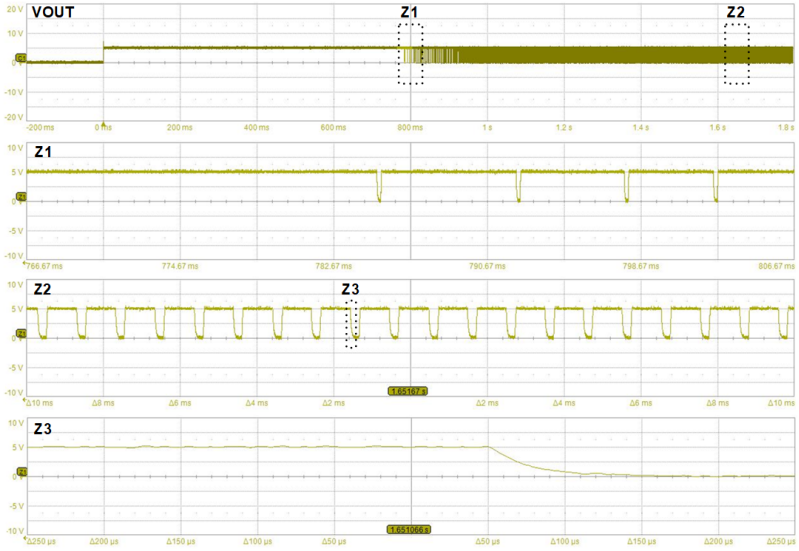

Fig. 14. Measured dynamic behavior of the VOUT (before and during multiple OTP events – first plot). The second plot represent a zoom in around the time of the first OTP event (Z1). The third plot embody a zoom in the area when the thermal stability was reached (Z2) and the forth plot shows the VOUT behavior when an OTP event is triggered (Z3).

4. Summary and Conclusions

This paper has shown that even for a fairly well-known SC DC-DC topology the power dissipated within some of its circuitry could affect the robustness of the converter. This becomes an important issue in special operational conditions, such as full-load start-up and output shorted to ground. Three design options for implementing the OTP circuit were briefly discussed, then a design example was presented. A two-steps design methodology was introduced: a first-pass circuit was obtained by using standard, electrical-only simulations, then electro-thermal simulations were employed to choose the best location of the thermal sensor and to derive the resulting thermal coupling, thus allowing for adjusting the trip points of the OTP circuit.

The designed SC DC-DC converter was integrated in a standard CMOS process. Measurements performed on silicon included several tests that allowed for direct comparisons between electro-thermal simulations and testbench measurements. The good correspondence between simulations and measurements (less than 1% difference between the measured and simulated value of t_{2OTP}) validate the design methodology and demonstrate the need for OTP circuits even for relatively low-power SC DC-DC converters.

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References

[1] G. VILLAR PIQUE, H.J. BERVELD, E. ALARCON, *Survey and benchmark of fully integrated switching power converters: switched-capacitor versus inductive approach*, IEEE Transaction on Power Electronics, **28**(9), pp. 4156–4167, 2013.

[2] A. G. BAJENARU, C. BOIANCEANU and G. BREZEANU, *Investigation of electro-thermal behaviour of a linear voltage regulator and its protection circuits by simulator coupling*, CAS 2013 Int. Conference, Sinaia, pp. 237–240.

[3] FAN5602, *Universal step-up/step-down charge pump regulated DC/DC Converter*, Datasheet Fairchild Semiconductor, August 2009.

[4] M. BUDAES, L. GORAS, *Burst mode switched capacitor voltage converter modeling and design*, Romanian Journal of Information Science and Technology, **11**, 2008, pp. 347–366.

[5] H. LEE, P. MOK, *An SC Voltage Doubler with Pseudo-Continuous Output Regulation using a Three-Stage Switchable Opamp*, IEEE Journal of Solid-State Circuits, **42**(6), pp. 1216–1229, June 2007.

[6] L. SALEM, R. JAIN, *A Novel Control Technique to Eliminate Output-Voltage-Ripple in Switched-Capacitor DC-DC Converters*, IEEE Symposium of Circuits and Systems, 2011, pp. 825–828.

[7] B. R. GREGOIRE, *A Compact Switched-Capacitor Regulated Charge Pump Power Supply*, in IEEE Journal of Solid-State Circuits, **41**(8), pp. 1944–1953, Aug. 2006, doi: 10.1109/JSSC.2006.875303

[8] W. L. WALTER, *High-Eficiency, Low Noise, Inductorless, Step-down DC/DC converter*, United States Patent no. 6.438.005, 2002.

[9] B. R. GREGOIRE, *A Compact Switched-Capacitor Regulated Charge Pump Supply*, IEEE Journal of Solid-State Circuits, 41(8), pp. 1944–1953, August 2006.

[10] L. SALEM, P. MERCIER, *A battery-connected 24-ratio switched capacitor PMIC achieving 95.5% efficiency*, in proc. IEEE Symposium on VLSICircuits (VLSIC), 2015, pp. 340–341.

[11] C.-S. PLESA, M. NEAG, L. RADOIAS, *Design options for thermal shutdown circuitry with hysteresis width independent on the activation temperature*, Advances in Electrical and Computer Engineering, 17(1), 2017, pp. 69–74.

[12] M. PFOST, C. BOIANCEANU, H. LOHMEYER, M. STECHER, *Electrothermal simulation of self-heating in DMOS transistors up to thermal runaway*, IEEE Transactions on Electron Devices, **60**, 2013, pp 699–707.

[13] A.-G. BAJENARU, F. BALLARIN, C.M. BOIANCEANU, G. BREZEANU, *Extensive electro- thermal simulation methodology for automotive high power circuits*, PRIME Conference, 2014.