

# Effect of Silicon Surface Cleaning on Electrical Properties of As-Deposited Atomically Layer-Deposited (ALD) HfO<sub>2</sub> Films Obtained From Tetrakis(dimethylamino)Hafnium (TDMAH) and Water

Cornel COBIANU<sup>1, 2, \*</sup>, Florin NASTASE<sup>1, 2</sup>, Niculae DUMBRAVESCU<sup>1, 2</sup>, Octavian BUIU<sup>1, 2</sup>, Bogdan SERBAN<sup>1, 2</sup>, Mihai DANILA<sup>1</sup>, Raluca GAVRILA<sup>1</sup>, Octavian IONESCU<sup>1, 2</sup>, and Cosmin ROMANITAN<sup>1</sup>

<sup>1</sup>National Institute for Research and Development in Microtechnologies-IMT Bucharest, Romania

<sup>2</sup>Research Center for Integrated Systems, Nanotechnologies and Carbon-Based Nanomaterials (CENASIC)-IMT Bucharest, Romania

E-mail: [cornel.cobianu@imt.ro](mailto:cornel.cobianu@imt.ro)

**Abstract.** The paper presents the results of an experimental study of the electrical properties of ultrathin as-deposited HfO<sub>2</sub> films prepared at 200°C by atomic layer deposition (ALD) from the reaction between tetrakis(dimethylamino)hafnium (TDMAH) and water as function of silicon surface terminations. The comparison of high frequency C-V plots recorded on Al-HfO<sub>2</sub>-Si MOS capacitors prepared on Si-OH and Si-H terminated silicon and thermally annealed in nitrogen at 250°C have indicated a two-fold smaller oxide trapped charge, and a 5% higher effective dielectric constant (9.95) for capacitors prepared Si-OH with respect the same capacitors processed on Si-H terminated silicon. Weibull plots of the HfO<sub>2</sub> breakdown events at constant current injection through the dielectric as a function of charge to breakdown have revealed an increased reliability of the HfO<sub>2</sub> films deposited on Si-OH terminated silicon substrate, in terms of a much smaller number of early breakdown events and higher capability of carrying electrical charges, before failure. The results are explained in terms of reaction mechanism between TDMAH and silicon termination and its role on interface and bulk HfO<sub>2</sub> film properties.

**Key-words:** Atomic layer deposition, as-deposited HfO<sub>2</sub> films, hydrogenated and hydroxylated Si surface, breakdown field, C-V measurement, Weibull plots.

## 1. Introduction

The international roadmap for semiconductor technology has predicted that further scaling down of CMOS silicon technology much below 10 nm node will trigger the decrease of the equivalent oxide thickness below 1 nm and such an aggressive evolution will push the material research to gate oxides with a very high dielectric constant,  $k > 25$  [1]. Under these considerations, the quality of the gate dielectric and its chemical stability during post-deposition processing are essential, so that interlayer dielectrics formation at the interface between silicon and gate dielectric to be minimized and thus the  $k$  value to be preserved as high as possible [2].

For the control of the quality of the gate dielectric, silicon surface and its termination, very well controlled cleaning processes have been developed, where both the organic and metallic contaminants can be removed from the silicon surface [3]. Thus RCA-1 cleaning, consisting of 5 parts  $H_2O$ , 1 part 27% ammonium hydroxide ( $NH_4(OH)$ ) and 1 part 30% hydrogen peroxide ( $H_2O_2$ ) is used for removing organic residues from the silicon wafers. This cleaning procedure is creating an ultrathin silicon dioxide ( $SiO_2$ ) film on the silicon surface, due to its oxidation by the  $H_2O_2$  chemical attack on the Si surface. For the removal of the metallic contaminant, the RCA-2 cleaning is used, which is consisting of 6 parts of deionized water ( $H_2O$ ), 1 part 27% hydrogen chloride (HCl) and 1 part of hydrogen peroxide ( $H_2O_2$ ). This cleaning process is also creating an ultrathin film of silicon dioxide on the surface of silicon wafer. As the  $SiO_2$  film is hygroscopic, the silicon wafers cleaned by these two procedures will be thus hydroxyl terminated (Si-OH). In the case that a  $SiO_2$ -free surface is necessary before the next technological process, the silicon wafers which were cleaned by RCA-1 and RCA-2 procedures are further cleaned in a 2% HF dip solution ( $HF/H_2O=2\%$ ) which will remove this ultrathin  $SiO_2$  film and leave a hydrophobic silicon surface, which is Si-H terminated. This hydrophobic Si surface status will be preserved in ambient air for a limited time before the gate oxide fabrication. This was the situation for the CMOS technology where the thin  $SiO_2$  films were used as gate dielectrics, and this approach was constantly followed during entire scaling down process when the gate dielectric was continuously decreased with each technological node, up to a final value of about 3 nm. However, for such ultrathin gate dielectrics, high tunneling leakage currents started to appear [4]. Thus, the high- $k$  dielectrics like,  $Al_2O_3$  [5],  $ZrO_2$  [6],  $Ta_2O_5$  [7] and  $HfO_2$  [8] were considered for replacing the well-known  $SiO_2$  gate dielectrics. By using such high- $k$  dielectrics as gate dielectrics the gate capacitance value of the MOSFET transistor can be further preserved according to scaling down rules, while the thickness of the gate dielectric can be greater than 3 nm, *i.e.* above tunneling threshold. Thus, the major issue of an increased power consumption of the MOSFET transistors, due to the increased values of the gate leakage current can be eliminated.

This huge technological change in the MOSFET fabrication technology has brought a new interface under investigation, silicon-high  $k$  dielectrics, where physico-chemical instabilities due to solid-state chemical reactions at the interface between silicon and a high- $k$  dielectric are present. [9]. Such chemical reactions will occur during deposition of the high- $k$  dielectric layer as well as during further high thermal processes needed for the chip fabrication. Among the multiple methods used for the fabrication of the high- $k$  dielectrics films, like sputtering, electron gun evaporation or chemical vapor deposition (CVD), the atomic layer deposition (ALD) which is a derivation of CVD method, is one the most frequently used, due to its very strong control on the film thickness, its advanced step coverage features and low temperature operation [10].

The properties of the ALD  $HfO_2$  films used as gate dielectrics depend on the type of substrate, chemical precursors used for the layer formation, electrode used for contacting as well as on the thermal annealing to which the  $HfO_2$  film is exposed after deposition for finishing the fabrication

of the integrated circuit [11]. Earlier, we have presented for the first time the effect of the surface preparation on the dielectric properties of the as-deposited ALD films prepared from TMAH and water [12] and on the electrical charges from interface and effective dielectric constant [13].

It is the purpose of this paper to describe with more details the role of silicon surface termination on the reaction mechanism for the atomic layer deposition of HfO<sub>2</sub> films by the reaction between tetrakis(dimethylamino) Hafnium (TMAH) and water and to further correlate the electrical, dielectric and reliability properties of these as-deposited films with cleaning procedure and the associated Si-OH or Si-H terminations of the silicon surface .

## **2. Theoretical background related to Si-HfO<sub>2</sub> interface formation**

The mechanism of the HfO<sub>2</sub> film formation by the surface reaction between TMAH and water is presented below, where one can notice the important chemical composition differences at the Si-HfO<sub>2</sub> interface as a function of the silicon termination type. Specific to ALD deposition is the fact one monolayer of HfO<sub>2</sub> is obtained at the end of four process steps as follows:

First step: the TMAH precursor is flowing in the ALD reactor where it is fully adsorbed on the substrate surface and then reacts with the silicon termination, for the formation of the first “half-monolayer” of the future HfO<sub>2</sub> film.

Second step: A nitrogen purging process is taking place for removing any excess unreacted precursor and reaction products (like HN(CH<sub>3</sub>)<sub>2</sub>) between TMAH and silicon termination leaving a TMAH bonded by two of its four (Hf-N-(CH<sub>3</sub>)<sub>2</sub>) groups to the silicon substrate, with its specific chemical architecture depending on the termination type, hydroxylated or hydrogenated surface.

The result of these two process steps is the formation of the so-called half-reaction product bonded to the substrate as shown below. This half-reaction product is fully dependent on the silicon termination!

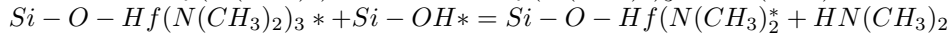
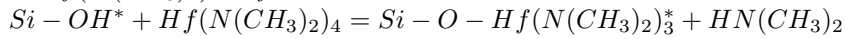
Third step: The water vapors are flowing in the ALD reactor and a reaction between H<sub>2</sub>O vapors and the remaining two unreacted (Hf-N-(CH<sub>3</sub>)<sub>2</sub>) groups of each TMAH molecule is taking place.

Fourth step: A nitrogen purging process is taking place for removing the reaction products between H<sub>2</sub>O vapors and “half-reacted” TMAH and the silicon substrate, with its specific chemical architecture depending on the termination type, hydroxylated or hydrogenated surface.

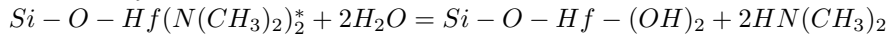
Below it is shown the specific chemical reaction mechanism for the first monolayer of HfO<sub>2</sub> film for each type of silicon termination.

### a) HfO<sub>2</sub> ALD film on OH-terminated Si surface

#### 1. *Hf(N(CH<sub>3</sub>)<sub>2</sub>)<sub>4</sub> half-reaction*

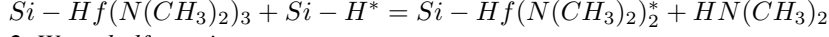
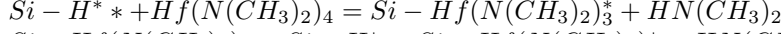


#### 2. *Water half-reaction*

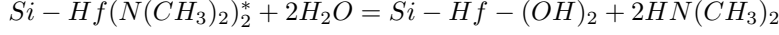


### b) HfO<sub>2</sub> ALD on H-Terminated Si Surface

#### 1. Hf(N(CH<sub>3</sub>)<sub>2</sub>)<sub>4</sub> half-reaction



#### 2. Water half reaction



From the above reaction mechanism, one can easily note that in the case of OH-terminated silicon surface, the Si-HfO<sub>2</sub> interface contains Si-O-Hf bonds, which preserves Si-O chemical bond specific to Si-SiO<sub>2</sub> interface, while in the case of Si-H terminated silicon surfaces, the Si-HfO<sub>2</sub> interface contains Si-Hf-O bonds which are probably much more favorable to further solid-state interface reactions in the subsequent thermal processes of the chip fabrication. Beyond the rather obvious differences between the Si-HfO<sub>2</sub> interface atomic architecture, as shown above, there may be differences related to the thermodynamic chemical favorability of the above TDMAH reactions with different silicon terminations, which may need further analysis. Such a thermodynamic modeling was done for the ALD HfO<sub>2</sub> films obtained by the reaction between tetrakis(ethylmethylamino)hafnium (TEMAH) and water precursors in the presence of the silicon substrate with Si-H or Si-OH termination [14]. Thus, by means of density functional theory (DFT), the authors have shown that the first half-reaction between TEMAH and hydroxylated silicon surface was exothermic by 1.65 eV with a small energy barrier of 0.1 eV. The second half reaction, *i.e.*, between the product of the first half reaction and the water had also a low activation energy, so overall the TEMAH-H<sub>2</sub>O reaction with Si-OH terminated silicon was thermodynamically favorable. On the other hand, the DFT modeling of the first half reaction between TEMAH and hydrogen terminated silicon surface has shown that this half-reaction was endothermic, with a high activation energy of 2.39 eV, while the second half-reaction went like in the case of Si-OH terminated silicon case.

This study has shown that from the thermodynamics point of view, probably higher temperatures may be needed for the ALD process during HfO<sub>2</sub> film formation on the hydrogenated silicon surfaces with respect to hydroxylated silicon surfaces. From such studies it can be speculated that the different compositional, structural and finally electrical properties of HfO<sub>2</sub> films may be obtained as a function of type of termination of silicon, at least in the as-deposited state of these HfO<sub>2</sub> films, and this was the final motivation for the experimental study which was performed within this paper.

## 3. Experimental

For this study, metal-oxide-semiconductor (MOS) capacitors were fabricated by using p-type (100) silicon wafer with electrical resistivity of (1-10) Ω\*cm. To obtain hydrogen terminated silicon wafers, an RCA-1 cleaning was applied, and this was followed by 2% HF dip. For reaching hydroxyl terminated Si wafer the following sequence of cleaning processes was used: RCA-1, followed by 2% HF dip solution, followed by RCA-2 solution. The HfO<sub>2</sub> film was prepared from TDMAH and water at a temperature of 200°C by using an “OpAL reactor” from Oxford Instruments.

The Al gate MOS capacitors with an area of 1\*10<sup>-4</sup> cm<sup>2</sup> were obtained by aluminum deposition, photolithography and etching, which was followed by a thermal annealing at only 250°C in nitrogen for 20 minutes, so that a minimum perturbation of the as-deposited state to occur.

The thickness of the HfO<sub>2</sub> film and of the bottom and upper interfaces of the film with silicon and air were measured on SmartLab XRD System from Rigaku by X-ray Reflectometry (XRR). The surface roughness of HfO<sub>2</sub> films was measured by an AFM Ntegra Auro from NT-MDT Spectrum Instruments. The high frequency C-V plots were recorded by Keithley 4200 Semiconductor Characterization System. The reliability characterization was performed on the same Keithley 4200 system by applying a constant current through the gate of MOS capacitor, with silicon biased in accumulation, and reading the time to breakdown and breakdown voltage. The charge to breakdown was obtained by multiplication of the time to breakdown by the applied constant current through the gate, with negative polarity of the voltage always on the Al gate so that the MOS capacitor to be biased in accumulation and thus the entire applied voltage to drop on the HfO<sub>2</sub> film and provide a real breakdown field of the dielectric films.

## **4. Results and Discussion**

Based on the differences in the atomic architecture of the Si-HfO<sub>2</sub> interface, where either Si-Hf-O or Si-O-Si chemical bonds are obtained at the end of the first HfO<sub>2</sub> monolayer formation, depending on hydrogen or hydroxyl termination, respectively, it is expected to see changes in the morphological and electrical properties of the ALD HfO<sub>2</sub> films used as gate dielectric in MOS capacitors, at least in the as-deposited state, and this is investigated below.

### **4.1. Morphological properties of as-deposited ALD HfO<sub>2</sub> film**

Very useful results were obtained by X ray reflectometry (XRR) which provided the thickness of the HfO<sub>2</sub>, film, the width of lower and upper interface of he HfO<sub>2</sub> film and the film gravimetric density, as shown in the Table 1 from below.

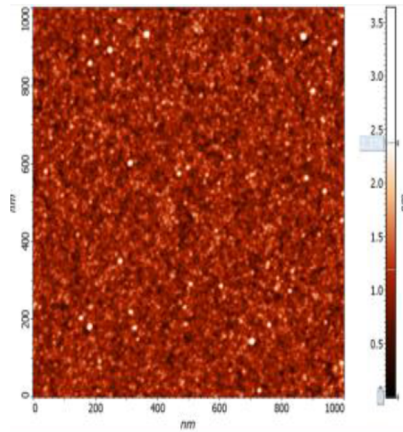
**Table 1.** XRR results obtained on as-deposited ALD HfO<sub>2</sub> films prepared on silicon with different termination

Cleaning process	RCA1+HF2%	RCA1+HF2% +RCA2
Si-HfO <sub>2</sub> interface width (nm)	0.3	0.33
HfO <sub>2</sub> film thickness (nm)	10.61±0.12	9.63±0.16
HfO <sub>2</sub> -air interface width (nm)	0.77±0.12	0.7±0.15
Film density (g/cm <sup>3</sup> )	8.09	8.67

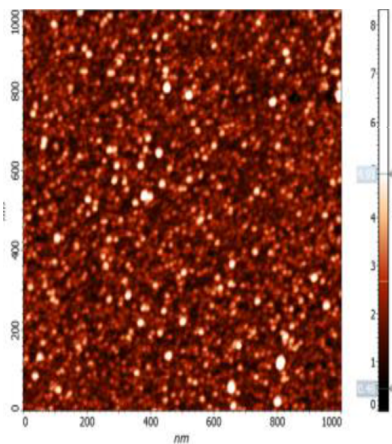
From this table, one can notice that the as-deposited Si-HfO<sub>2</sub> interface is very sharp, without any interlayer dielectric, and as predicted by the atomistic modelling, it may consist from the monolayer of Si-O-Hf atoms for the hydroxylated silicon (with RCA2 as the last cleaning step) and Si-Hf-O for the hydrogenated interface. The fact that the interface width is larger for the hydroxylated surface of silicon may be overall correlated with more than one monolayer of SiO<sub>2</sub> at the interface due to oxidation created by H<sub>2</sub>O<sub>2</sub> in the last cleaning step of the RCA2. On the other hand, the relatively wider outer HfO<sub>2</sub>-air interface with respect to bottom interface may be correlated with a higher chemical non-homogeneity towards air, due to possible carbon and humidity adsorption on the top of the HfO<sub>2</sub> layer. A very useful result of XRR analysis is the value of gravimetric density as a bulk information. The difference between the two gravimetric density values, 8.09 g/cm<sup>3</sup> for hydrogen terminated silicon substrate versus 8.67 g/cm<sup>3</sup> for hydroxylated silicon surface is important and it shows rather unexpected high influence of the atomic arrangement at the interface to the atomic network within entire body of the as-deposited HfO<sub>2</sub> film.

Overall, the  $\text{HfO}_2$  film deposited on hydroxylated silicon surface is denser than that prepared on hydrogenated Si surface, and this may impact other bulk properties of the as-deposited film, like in the case of dielectric constant, where any air inclusion in the film may decrease the value of this “k” parameter. This correlation will be further investigated below.

Figs. 1 and 2, show the results of the morphological characterization of the surface of the  $\text{HfO}_2$  films prepared under identical conditions excepting the silicon termination, as described above. Thus, Fig. 1 reveals the root mean square equal to 0.26 nm (RMS) for the surface roughness of the  $\text{HfO}_2$  films deposited on hydrogen terminated silicon, while Fig. 2 presents an RMS value equal to 0.76 nm recorded on the  $\text{HfO}_2$  films deposited on hydroxyl terminated silicon surface. Such RMS value may give an indication about the surface roughness of the starting silicon surface, at the end of different chemical cleaning processes, which is then replicated at the upper surface of  $\text{HfO}_2$  film due to the excellent step coverage of the ALD process, as described above.



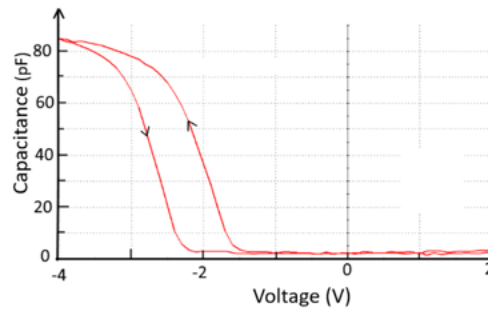
**Fig. 1.** AFM on ALD  $\text{HfO}_2$  film deposited on Si-H surface. RMS=0.26 nm. Ref. [12].



**Fig. 2.** AFM on ALD  $\text{HfO}_2$  film deposited on Si-OH surface. RMS=0.76 nm. Ref. [12]

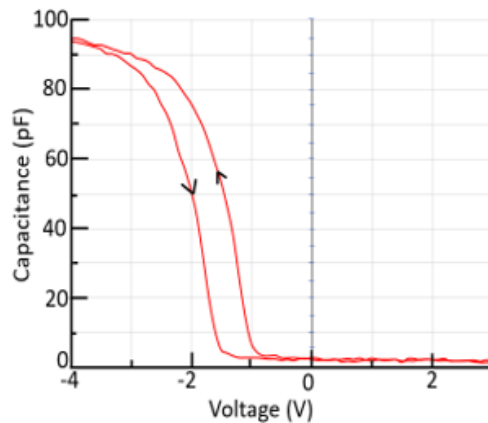
#### 4.2. Electrical properties of as-deposited HfO<sub>2</sub> films

For the evaluation of the electrical charges at the interface and in the bulk of the HfO<sub>2</sub> films, the high frequency C-V plots were performed on MOS capacitors prepared on silicon substrates with both types of terminations [13]. Thus, in Fig. 3, it is shown the typical dual voltage sweep C-V plot recorded at 1 MHz for the MOS capacitor processed on hydrogen terminated silicon, with a thickness of the ALD HfO<sub>2</sub> film of 10.61 nm. As indicated in Fig. 3, the measurement has started at a gate voltage of +2V and returned to this value. This dual voltage sweep has allowed the extraction of the oxide trapped charge [15], as it will be shown later.



**Fig. 3.** Dual voltage sweep C-V plot for a MOS capacitor processed on hydrogen terminated p-type silicon, with as-deposited HfO<sub>2</sub> film (10.61 nm), Al gate annealed at 250°C. Ref. [13].

In Fig. 4, similar measurements are shown but on MOS capacitors processed on hydroxylated silicon substrate, while the thickness of the ALD HfO<sub>2</sub> film was 9.63 nm.



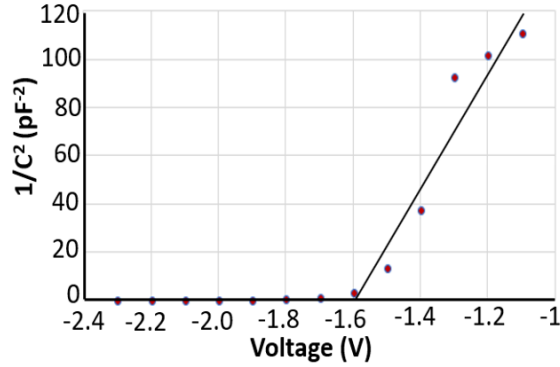
**Fig. 4.** Dual voltage sweep C-V plot for a MOS capacitor processed on hydroxyl terminated p-type silicon, with as-deposited HfO<sub>2</sub> film (9.63 nm), Al gate annealed at 250°C. Ref. [13].

From these high frequency C-V plots one can extract the flatband voltage (VFB), the effective dielectric constant of the as-deposited HfO<sub>2</sub> film ( $k_{eff}$ ), the fixed charge from the interface Si-HfO<sub>2</sub> and the electrical charge trapped in the oxide. The flatband voltage was calculated from the Mott-Schottky equation (1) from below [16].

$$1/C^2 = (2/(\varepsilon_0 \varepsilon_{Si} A^2 e N_A))(V - V_{FB} - k_B T/e), \quad (1)$$

where  $\varepsilon_0$  is the dielectric permittivity of vacuum,  $\varepsilon_{Si}$  is the dielectric constant of silicon,  $A$  is the area of the MOS capacitor,  $N_A$  is the acceptor ion concentration in silicon,  $k_B$  is the Boltzmann constant,  $T$  is the ambient temperature in Kelvin degrees and “ $e$ ” is the electron charge.

By representing the equation (1) as a function of voltage, as it is shown in Fig. 5, one can notice that the plot  $1/C^2$  intercepts the voltage axis at the value  $V = V_{FB} + k_B T/e$ , and thus, from this intercept, the flatband voltage can be extracted. Based on this approach, the flat band voltage was determined for each sweep direction. Thus,  $V_{FB1}$  is associated to C-V plot characterized by voltage sweep from inversion to accumulation and  $V_{FB2}$  is associated to voltage sweep from accumulation to inversion, while  $\Delta V_{FB} = V_{FB2} - V_{FB1}$ . The values of  $V_{FB1}$ ,  $V_{FB2}$  and  $\Delta V_{FB}$  were calculated for five MOS capacitors performed on Si-H terminated silicon and Si-OH terminated silicon substrates as shown in Tables 2 and 3, respectively. In the same tables, one can also find the effective dielectric constants,  $k_{eff}$ , of the  $HfO_2$  films deposited on the two types of silicon terminations.



**Fig. 5.** Mott-Schottky plot for the extraction of the flatband voltage of MOS capacitor with as-deposited  $HfO_2$  as dielectric. Ref. [13].

These values of  $k_{eff}$  were calculated by using the high frequency MOS capacitance ( $C_{ox}$ ) in accumulation, at  $V_G = -3.5V$ , as follows.

$$C_{ox} = \varepsilon_0^* k_{eff}^* A/d \quad (2)$$

where  $A$  is the area of the capacitor and  $d$  is the thickness of the  $HfO_2$  film. From formula (2) one can easily understand that an effective dielectric constant is associated to the entire thickness,  $d$ , even if there may be one or two monolayers of  $SiO_x$  at the interface between silicon and  $HfO_2$  film, like in the case of silicon substrate cleaned in RCA1-2%HF-RCA2. Such interface layer, with a dielectric constant around 4 will decrease the high  $k$  capabilities of the entire gate dielectric film.

Therefore, the effective dielectric constant,  $k_{eff}$ , of  $HfO_2$  film calculated by this formula is underestimating the real value of the dielectric constant of  $k_{eff}$ , but for the  $HfO_2$  thickness of about 10 nm, the error is less than 10%. However, from the application point of view, this  $k_{eff}$  value is what it matters, so it is correct to operate with this value.

**Table 2.** Parameters of MOS capacitors performed on Si-H terminated silicon, specific to as-deposited ALD HfO<sub>2</sub> films. Ref. [13]

Chip #	1	2	3	4	5
Cox (pF)	83.46	80	80	79.47	79.7
V <sub>FB1</sub> (V)	-1.6	-1.3	-1.3	-1.3	-1.1
V <sub>FB2</sub> (V)	-2.5	-2.3	-2.3	-2.3	-1.2
ΔV <sub>FB</sub> (V)	-0.9	-1	-1	-1	-1.2
k <sub>eff</sub>	10	9.6	9.6	9.52	9.55
N <sub>f</sub> (cm <sup>-2</sup> ) x 10 <sup>12</sup>	4	2.1	2.1	2.09	1.1
N <sub>ot</sub> (cm <sup>-2</sup> ) x 10 <sup>12</sup>	4.69	5	5.25	4.96	5.97

**Table 3.** Parameters of MOS capacitors performed on Si-H terminated silicon, specific to as-deposited ALD HfO<sub>2</sub> films. Ref. [13]

Chip #	1	2	3	4	5
Cox (pF)	92.6	91.55	91.65	91.48	91.34
V <sub>FB1</sub> (V)	-1	-1.2	-1.1	-1.05	-1.27
V <sub>FB2</sub> (V)	-1.5	-1.7	-1.65	-1.55	-1.65
ΔV <sub>FB</sub> (V)	-0.5	-0.5	-0.55	-0.5	-0.38
k <sub>eff</sub>	10.1	9.96	9.97	9.95	9.94
N <sub>f</sub> (cm <sup>-2</sup> ) x 10 <sup>12</sup>	0.7	1.83	1.26	0.9	2.23
N <sub>ot</sub> (cm <sup>-2</sup> ) x 10 <sup>12</sup>	2.9	2.9	3.15	2.85	2.16

In the above tables, the fixed charge from the Si-HfO<sub>2</sub> interface was calculated by using the formula from below [15].

$$N_f = (\Phi_{Al-Si} - V_{FB1}) C_{ox} / (e A) \quad [cm^{-2}] \quad (3)$$

where  $\Phi_{Al-Si}$  is equal to  $-0.88V$  and corresponds to work function difference between Al gate and (100) boron doped p-type silicon with doping concentration  $N_A = 10^{15} \text{ cm}^{-3}$ , while  $C_{ox}$  is the capacitance of the MOS device biased in accumulation.

In the above tables, it is also calculated the charge trapped in the HfO<sub>2</sub> oxide during dual voltage sweep by means of the high frequency MOS characteristics and the formula is given below [15].

$$N_{ot} = -\Delta V_{FB} C_{ox} / (e A) \quad [cm^{-2}] \quad (4)$$

where  $\Delta V_{FB} = V_{FB2} - V_{FB1}$ . The trapped charge in the oxide,  $N_{ot}$  is caused by the net injected charge in the oxide during voltage sweep. This trapped charge could be located inside the bulk of the HfO<sub>2</sub> film, but the most important contribution to the shift of the C-V plots will come from the trapped charge which remained near the Si-HfO<sub>2</sub> interface.

The results from Tables 2 and 3 show a rather low dielectric constant ( $k_{eff}$  of about 10 for films deposited on Si-OH terminated silicon, and a  $k_{eff}$  of 9.6 for the as-deposited HfO<sub>2</sub> films deposited on Si-H terminated silicon), as they are extracted from the high frequency accumulation capacitance of the Al gate-MOS capacitors annealed at only 250°C in nitrogen. The higher

values of  $k_{eff}$  obtained for the HfO<sub>2</sub> film deposited on hydroxylated silicon (Table 3) with respect to the same film deposited on hydrogenated silicon (Table 2) cannot be simply explained by the fact that those former layers are thinner and therefore their capacitance is higher which will increase the value of dielectric constant as per equation (2). The fact that a higher value of  $k_{eff}$  was obtained in the presence of a SiO<sub>x</sub> interlayer at the interface, which actually is decreasing the overall value of  $k_{eff}$  may be also supported by the higher gravimetric density of the HfO<sub>2</sub> films deposited on Si-OH terminated silicon (Table 1), which will render a higher compactness of those films, eliminating thus the effect of porosity, where air can also decrease the overall dielectric constant of a HfO<sub>2</sub> film. Therefore, it is expected that even for the same thickness of the as-deposited HfO<sub>2</sub> films deposited on Si-OH terminated and Si-H terminated silicon, a higher value of  $k_{eff}$  to be obtained on the former due to increased gravimetric density of HfO<sub>2</sub> films deposited on Si-OH terminated silicon. However, all these results show that further film optimization is needed by both deposition kinetics research and further thermal annealing which will occur during further processing of the integrated circuit.

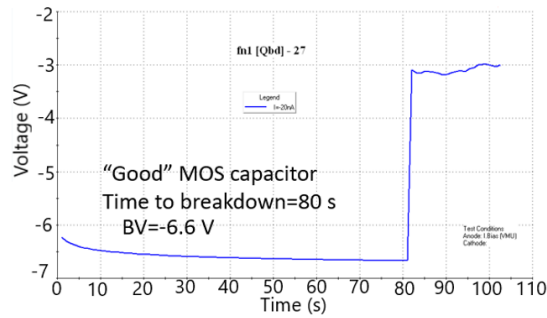
From the inspection of the Figs. 3 and 4, it is observed that the C-V plots are shifted to negative voltages and this is an indication that a positive charge is residual in the as-deposited HfO<sub>2</sub> films, near the interface with silicon, and this charge is higher in the films deposited on Si-H terminated films. Even if there is some dispersion between the  $N_f$  values extracted from different MOS chips in Tables 2 and 3, overall, it can be accepted the result that fixed charge at the interface,  $N_f$  is much smaller in the HfO<sub>2</sub> films deposited on Si-OH terminated silicon, where a SiO<sub>x</sub> film is present with respect to HfO<sub>2</sub> films deposited on Si-H terminated films, where a Si-Hf-O atomic arrangement was theoretically found. Thus, the robust Si-SiO<sub>2</sub> interface, which assured the success of the IC technology in the last six decades, has shown again its benefic effect, even here the SiO<sub>x</sub> oxide was the result of a cleaning process.

From Figs. 3 and 4 and Tables 2 and 3 one can also notice that the flatband voltages  $V_{FB1}$  and  $V_{FB2}$  obtained at the end of the dual voltage sweep are both smaller for the MOS capacitors prepared on Si-OH terminated silicon, which will also provide almost two-times smaller values for the charge trapped in the oxide due to the dual voltage sweep, showing again a much more robust interface for the Si-HfO<sub>2</sub> in the presence of one or two SiO<sub>x</sub> monolayers at the interface, even if this interface layer was the result of a cleaning process in H<sub>2</sub>O<sub>2</sub>.

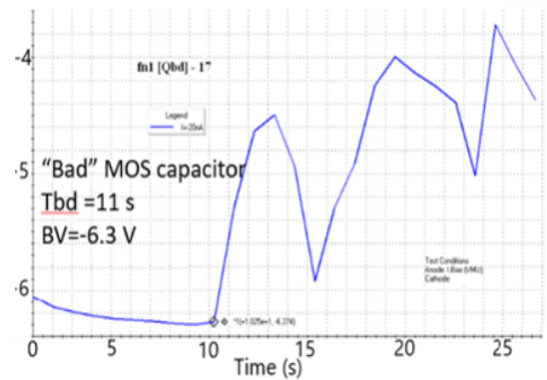
To further explore the differences between these two types of as-deposited HfO<sub>2</sub> films, a reliability investigation is shown below.

### 4.3. Reliability of as-deposited ALD HfO<sub>2</sub> films

For the reliability study of the as-deposited HfO<sub>2</sub> films deposited on silicon wafers with different terminations, breakdown characteristics were measured on fresh MOS capacitors, biased with silicon in accumulation, *i.e.* the negative polarity of the voltage to be on the aluminum gate, which is equivalent to electron injection from the gate.



**Fig. 6.** Time to breakdown and breakdown voltage for a good MOS capacitor with as-deposited ALD HfO<sub>2</sub> as dielectric. Injected constant current= $I=20$  nA.

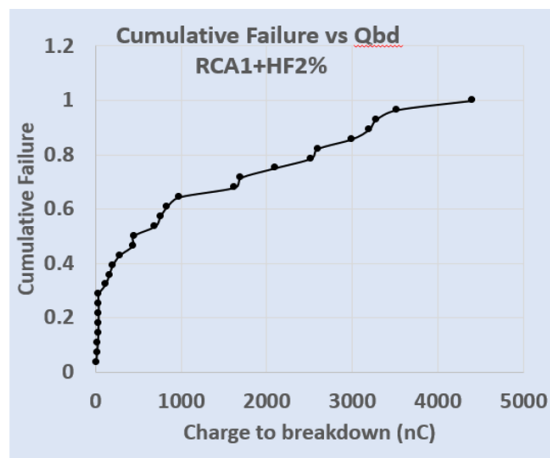


**Fig. 7.** Time to breakdown and breakdown voltage for a bad MOS capacitor with as-deposited ALD HfO<sub>2</sub> as dielectric. Injected constant current= $I=20$  nA.

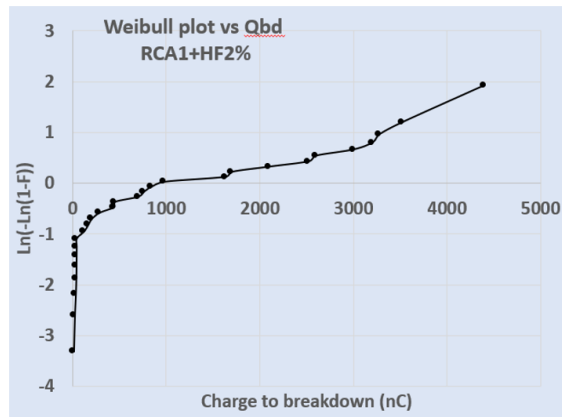
For this purpose, a constant current of 20 nA was injected through the gate of each MOS capacitors and the time to breakdown ( $T_{bd}$ ), the charge to breakdown ( $Q_{bd}$ ), the breakdown voltage ( $V_b$ ) and the breakdown field ( $E_{bd}$ ) were recorded for that device [17]. The charge to breakdown is simply obtained by multiplying the time to breakdown with constant current ( $I$ ) injected through the aluminum gate. This procedure is shown in Figs. 6 and 7, where typical time-to-breakdown results are shown. From these figures one can see the definition of the breakdown event when the MOS capacitor is excited in constant current. Thus, Fig. 6 indicates that HfO<sub>2</sub> dielectric breakdown event appears when the voltage corresponding to the injected constant current, of about -6.5 V, is no longer supported by the capacitor and its value drastically decreases to about -3 V. At that voltage condition, the capacitor failed and then this is behaving like poor resistor. Fig. 7 presents a breakdown event where the capacitor shows initially the trend to self-heal for a short time, but then finally this will collapse. The time to breakdown for this capacitor was the moment when the voltage has the first jump to -4.5 V. The slight increase of the voltage on capacitor during constant current injection through the HfO<sub>2</sub> dielectric is associated with the generation of new traps in the dielectric. The charge trapping in these new traps creates an electric field which is opposite to the electric field due to applied constant current, and therefore for preserving the constant current through the MOS capacitor, the voltage on the capacitor

increases for compensating the internal electric field. From Figs. 6 and 7, one can easily note that a major difference in the time to breakdown can appear for the two capacitors, which have a similar breakdown voltage. This result demonstrates the ability of the  $T_{bd}$  and  $Q_{bd}$  methods to correctly discriminate the quality of two MOS capacitors by means of their capability to carry a certain amount of charge before breakdown, even when the value of breakdown voltage is almost the same.

To evaluate the breakdown properties of the MOS capacitors performed on silicon substrate with different terminations, in Figs. 8 and 9, the cumulative failure distribution and the associated Weibull plots are shown for the MOS capacitors prepared on Si-H terminated silicon, while in Figs. 10 and 11, the similar results are presented for MOS capacitors performed on Si-OH terminated silicon.



**Fig. 8.** Cumulative failure distribution (F) as a function charge to breakdown for 30 MOS capacitors with ALD HfO<sub>2</sub> film (10.61 nm) deposited on Si-H terminated silicon, Ref. [12].

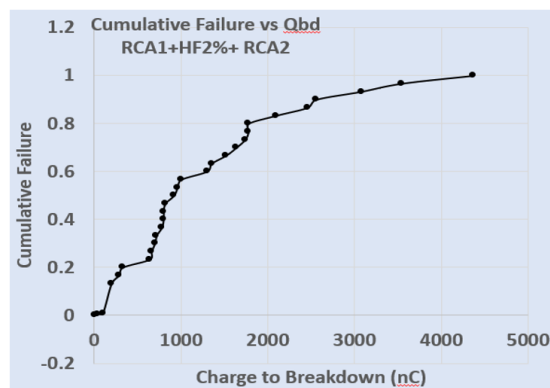


**Fig. 9.** Weibull plot as a function of charge to breakdown for 30 MOS capacitors with ALD HfO<sub>2</sub> film (10.61) deposited on Si-H terminated silicon, Ref. [12].

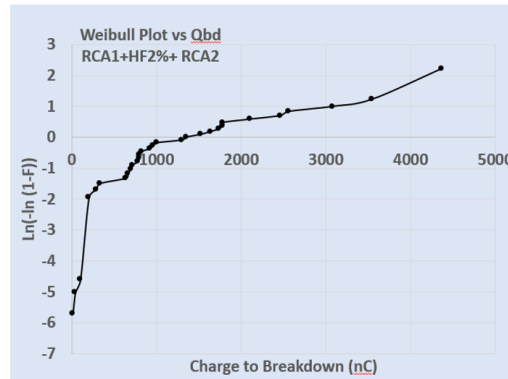
For obtaining these results, 30 breakdown events of MOS capacitors with HfO<sub>2</sub> film as a dielectric were recorded from different places on the wafer with the same type of silicon termination. Then the breakdown events were ordered and the cumulative failure distribution from Fig. 8 was obtained by counting the number breakdown events (F) which occurred up to a certain value of the charge to breakdown. By knowing the cumulative failure distribution as a function of  $Q_{bd}$ , the Weibull plot from Fig. 9 was then obtained [18].

From both Fig. 8 and 9, it is noticed that there is an increased number of early breakdowns for the capacitors fabricated on Si-H terminated silicon. In fact, for MOS capacitors fabricated on Si-H terminated silicon, more than 40% of these capacitors have had an early breakdown at  $Q_{bd} < 200$  nC. The advantage of Weibull distribution for dielectric breakdown in MOS capacitors consists in the fact that from a limited number of charge-to-breakdown events, one can understand the behavior of the charge to breakdown (correlated to lifetime at a certain constant current injection) of the device and one can also infer the transition from defect related breakdown to the intrinsic breakdown mechanism. Thus from Fig. 9, and the mathematical features of Weibull distribution, where intercept of x-axis occurs at  $F=63.2\%$ , one can easily infer that 63.2% of the dielectric breakdown events take place for the charge to breakdown up to 1000 nC. On the other hand, the small slope of the Weibull distribution towards the highest values of charge to breakdown of 4400 nC indicates that the intrinsic breakdown was not reached for these broken devices. This result may suggest that the capacitor area of  $100 \text{ cm}^{-2}$  ( $100 \mu\text{m} \times 100 \mu\text{m}$ ) may be too high and therefore the probability to have a killing defect on each capacitor is equal to 1.

From the results shown in Figs. 10 and 11 one can see that the number of the early breakdown events is much reduced. Thus, with respect to the capacitors prepared on Si-H terminated silicon, only 20% of the MOS capacitors fabricated on Si-OH terminated silicon had an early breakdown at  $Q_{bd} < 200$  nC. In addition, according to Fig. 11, the  $Q_{bd}$  limit increased from 1000 nC to 1300 nC at the intercept of Weibull function with the x axis.



**Fig. 10.** Cumulative failure distribution, F, as a function of charge to breakdown for 30 MOS capacitors with ALD HfO<sub>2</sub> film (9.63 nm) deposited on Si-OH terminated silicon, Ref. [12].



**Fig. 11.** Weibull plot as a function of charge to breakdown for 30 MOS capacitors with ALD HfO<sub>2</sub> film (10.61) deposited on Si-H terminated silicon, Ref. [12].

From the small slope of the Weibull plot at high values of the  $Q_{bd}$  in Fig. 11, one can prove that the breakdown mechanism in HfO<sub>2</sub> films deposited on Si-OH terminated silicon is again defect related on the entire range  $Q_{bd}$  values.

By comparing the breakdown results of the HfO<sub>2</sub> films deposited on Si films with Si-H and Si-OH terminations, one can show that, overall, the reliability of the HfO<sub>2</sub> film can be influenced by the type of silicon termination. The reduced number of early breakdown events on the Si-OH terminated silicon may be explained in terms of a smaller number of defects responsible for this type of breakdown, which could be correlated with a more compact film as revealed by XRR, a chemically stronger interface of Si-O-Hf atomic arrangement with respect to Si-Hf-O, and an easier nucleation process for the HfO<sub>2</sub> films deposited on Si-OH terminated silicon, due to the overall exothermic reaction between TMAH and hydroxylated silicon, as described above.

Moreover, the fact one or two monolayers of SiO<sub>x</sub> films were present at the interface of the Si-HfO<sub>2</sub> due to the RCA1-2%HF-RCA2 cleaning have had a benefic effect on the electrical and dielectric properties of as-deposited HfO<sub>2</sub> films, even if such SiO<sub>x</sub> interlayer can decrease the overall dielectric constant of the HfO<sub>2</sub> film. Future work is necessary to evaluate the effect of further thermal processes on the evolution of the interface and bulk properties of the HfO<sub>2</sub> films as function of the initial termination of the silicon substrate.

## 5. Conclusions

The electrical and dielectric characterization of the as-deposited atomically layer deposited HfO<sub>2</sub> films prepared from tetrakis(dimethylamino) hafnium (TDMAH) and water at 200°C on silicon substrate with Si-H or Si-OH termination has indicated improved interface (charges and more stable atomic architecture) and bulk properties (trapped charges in the oxide, gravimetric density and effective dielectric constant) of the HfO<sub>2</sub> films deposited on hydroxylated silicon substrates.

The high frequency C-V characterization of the as-deposited HfO<sub>2</sub> film prepared on silicon with Si-H and Si-OH terminations have shown an almost half amount of charge trapped in the oxide for the HfO<sub>2</sub> films on Si-OH terminated silicon with respect to as-deposited HfO<sub>2</sub> films on Si-H terminated silicon, while the effective dielectric constant was incrementally higher for films

deposited on hydroxylated silicon (9.95) with respect to  $k_{eff}=9.6$  on hydrogenated silicon), even if an SiO<sub>x</sub> interlayer was present for the films deposited on hydroxylated Si substrate.

The dielectric breakdown characterization expressed in charge to breakdown of the as-deposited HfO<sub>2</sub> films has shown that the number of early breakdown events was two times lower for the films deposited on Si-OH terminated silicon substrate.

These results were explained in terms of the existence of a SiO<sub>x</sub> (mono)layer, and a Si-O-Hf atomic architecture present at the interface of the Si-OH terminated silicon determining the kinetics of nucleation process on hydroxyl terminated silicon substrate, which may have also influenced the bulk properties of the as-deposited HfO<sub>2</sub> film formation, as revealed by the higher gravimetric density and compactness of the later HfO<sub>2</sub> films.

The overall keff value of the as-deposited HfO<sub>2</sub> films was rather low suggesting that further optimization of the film deposition and annealing may be necessary for its application to next generations of silicon integrated circuits.

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