

Charge retention of a Floating gate Transistor for a Reset Controller

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Abstract. An integrated reset controller (voltage supervisor) is designed and implemented. The system generates a reset signal, active while power supply brownout conditions are detected and for 250 ms after the supply voltage has increased to acceptable levels. The circuit is built in a *Deep N-Well* (DNW) 5V 0.35 μ m CMOS process, which provides good isolation between the on-chip devices and the substrate. The controller is based on a comparator, which uses a programmable voltage reference built with *Floating Gate* (FG) transistors. The voltage supervisor's operation is demonstrated by simulations and measurements. The charge retention capability of the FG transistors is analyzed, using the Arrhenius model to estimate behavior under normal operating conditions, based on its behavior at high temperatures.

Key-words: On-Chip Isolation, Deep N-Well, Reset Controller, Programmable Voltage Reference, Floating Gate Transistors, Charge Retention, Arrhenius Model.

1. Introduction

Deep sub-micron processes provide an opportunity for low cost, very large scale integration of mixed signal functions on the same chip [1, 2]. A significant technical challenge in IC design is on-chip isolation, which is becoming increasingly important due to higher integration levels at high working frequencies [1, 2]. The *Deep N-Well* (DNW) is an n-type layer buried inside the epitaxial layer used in CMOS technologies. The addition of this layer is used to improve transistors isolation and reduce substrate noise coupling in mixed-signal circuits [3].

Another technology with improved on-chip isolation is the *Silicon-On-Insulator* (SOI) process. SOI has many advantages, such as lower parasitic capacitances and higher immunity to

latch-up problems [3]. However, an important limitation of this technology is the high cost, which is not the case for the DNW process.

This paper presents the implementation of a reset controller in a Deep N-Well process. These voltage supervisors are employed in many applications to monitor the power supply of the system. Supervising the power rails is essential for digital and mixed-signal architectures, in order to protect the component logic circuits when a brownout occurs [3, 4].

The proposed voltage supervisor contains a non-volatile programmable reference voltage implemented with FG transistors, used for determining the power supply threshold [4]. By implementing the reset controller in a DNW process, the voltage required for programming the voltage reference is reduced, which is a significant benefit in the case of low voltage ICs.

High reliability is required from systems that could cause injury if they malfunction. One of those failures could be a supply voltage drop for a limited period of time, which needs to be detected by the reset controller (even after years of operation). The power supply threshold's variation in time is related to the reliability of the floating gate transistors with which the programmable reference is built. The most crucial aspect of FG reliability for this application is thus the charge retention on the floating gate [5] (the transistor's threshold voltage is determined by the charge on the FG). The charge retention is investigated experimentally in this paper, based on the Arrhenius model.

2. DNW process description

The DNW process architecture is shown in Fig. 1. The Deep N-Well layer is connected to the n-well and creates two vertical PN junctions: one with the formed isolated p-type region in the surface (p- isolated, Fig.1) and the other with the substrate below. The DNW layer is connected to the power supply (V_{DD}) through the n+/n-well sinks, while the p-type isolated region is connected to ground (GND). The p- substrate is also tied to GND, in the standard DNW process.

In the case of the reset controller described in this paper, a different substrate connection is proposed. Due to packaging and design considerations, the p-substrate is coupled to (V_{DD}). As a consequence, all of the circuit devices are built within the p- isolated region (Fig.1).

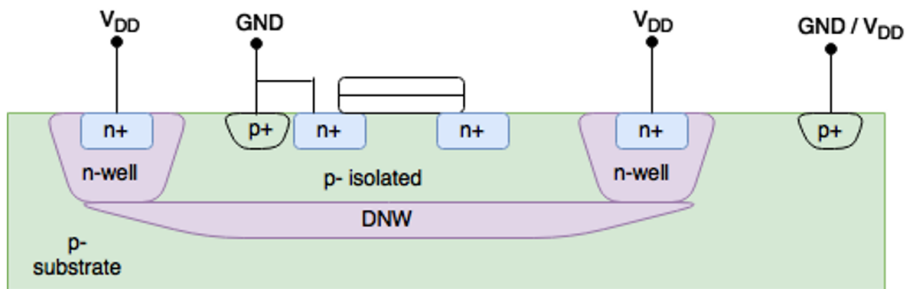


Fig. 1.: Cross section of a Deep N-Well Process.

The reset controller pin-out requires that the lead frame be connected to (V_{DD}). The DNW itself is also tied to the power supply voltage, thereby shorting the parasitic substrate-well diode. Note that in a previous circuit implementation, the die, built on a p-type substrate with no DNW, was attached to the lead frame using an insulating resin. This was a cost ineffective solution.

Furthermore, the implementation of the reset controller in the described DNW process also allows for a negative V_{ss} voltage to be applied. This voltage is only used at the wafer level, while the circuit is in test mode.

3. Charge Retention in Floating Gate Devices

A floating gate transistor, shown in Fig. 2, has an additional gate electrode, which is completely surrounded by dielectric. Being electrically isolated, this floating electrode can be used to store charge, which makes the FG transistor a device with memory [6].

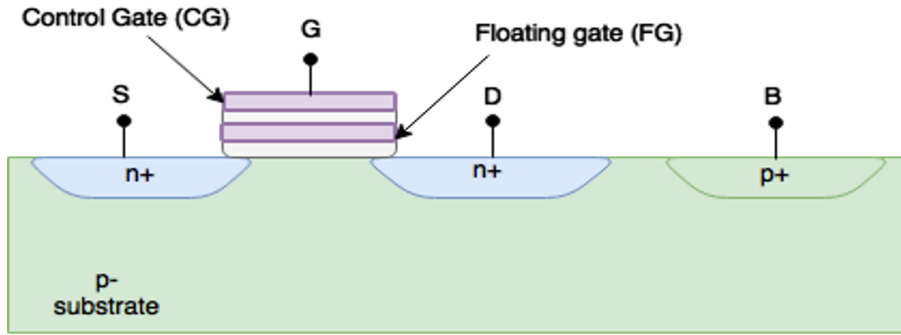


Fig. 2.: Cross section of a Floating Gate (FG) transistor.

The phenomenon utilized for programming the floating gate charge is Fowler-Nordheim tunneling [6, 7]. If the floating gate is not charged then the device behaves like a normal n-type MOSFET. A positive charge stored in the floating gate leads to the formation of an inversion channel in the p-substrate region (Fig. 2). If the floating gate is negatively charged, then this charge shields the channel region from the main control gate (CG) and prevents the formation of a connection between source and drain [7].

The distinguishing characteristic of the FG transistor is that its threshold voltage (V_{TH}) can be controlled via the charge stored on the floating gate. An important feature of FG reliability is correlated to charge retention on the floating gate [5]. Charge retention is defined by the ability of the FG device to retain charge over long periods of time regardless of whether the part is powered on or powered off [8–12].

Retention capability is analyzed by applying a thermal treatment (wafer level bake) after programming the FG cell, which increases the natural rate at which the floating gate charge varies through dielectric leakage [9–11]. By studying charge retention in this accelerated experiment, the storage capabilities under normal operating conditions can be determined, using this formula:

$$t_{USE} = AF \cdot t_{STRESS} \quad (3.1)$$

where:

- t_{USE} is the use time at room temperature under normal operating conditions,
- AF is the acceleration factor,
- t_{STRESS} is the stress time (the duration of the high temperature treatment).

A rate coefficient (R) can be defined as the inverse value of time. Thus, t_{STRESS} and t_{USE} are equal to $1/R_{STRESS}$ and $1/R_{USE}$ respectively. In this manner, the acceleration factor from (3.1) can be expressed as:

$$AF = \frac{R_{STRESS}}{R_{USE}} \quad (3.2)$$

The rate coefficient is calculated using the Arrhenius model, which is an industry standard for estimating retention for floating gate devices [5, 8, 9]. This model is based on a theoretical relationship between chemical reaction rates and temperature and is expressed by the formula:

$$R = A \cdot \exp\left(-\frac{E_A}{kT}\right) \quad (3.3)$$

where:

- A is a constant [s^{-1}],
- E_A is the activation energy [KJ/ mol],
- k is Boltzmann's constant [$K = 8.314 \cdot 10^{-3}$ KJ/ mol K],
- T is temperature [K].

It can be observed in (3.3) that the rate coefficient varies with temperature and the activation energy. The Arrhenius model is used to find the acceleration factor between a stress temperature and a normal usage condition, which in turn can be used to de-rate results from an accelerated stress test. If (3.3) is taken into consideration, (3.2) can be written as:

$$AF = \frac{A \cdot \exp\left(\frac{E_A}{kT_{STRESS}}\right)}{A \cdot \exp\left(-\frac{E_A}{kT_{USE}}\right)} = \exp\left(\frac{E_A}{kT_{USE}} - \frac{E_A}{kT_{STRESS}}\right) \quad (3.4)$$

where T_{USE} is the use temperature [K] and T_{STRESS} is the stress temperature [K].

The acceleration factor becomes:

$$AF = \exp\left[\frac{E_A}{k} \left(\frac{1}{T_{USE}} - \frac{1}{T_{STRESS}}\right)\right] \quad (3.5)$$

Based on relations (3.5) and (3.1), the Arrhenius model shows that a higher temperature applied for a shorter time is equivalent to a larger duration under normal use (if T_{STRESS} is greater than T_{USE} , $AF > 1$, therefore $t_{USE} > t_{STRESS}$).

Considering a typical activation energy $E_A = 77.1$ kJ/mol [9], with the stress temperature at 225°C ($T_{STRESS} = 523\text{K}$), and the use temperature at 27°C ($T_{USE} = 300\text{K}$), for a stress time $t_{STRESS} = 24$ hours ($R_{STRESS} = 1.15 \cdot 10^{-5} s^{-1}$), the use time t_{USE} is 630 years, being obtain using formulas (3.1) and (3.5). Equivalent use time values for several stress times were obtained in the same manner and are given in Fig.3.

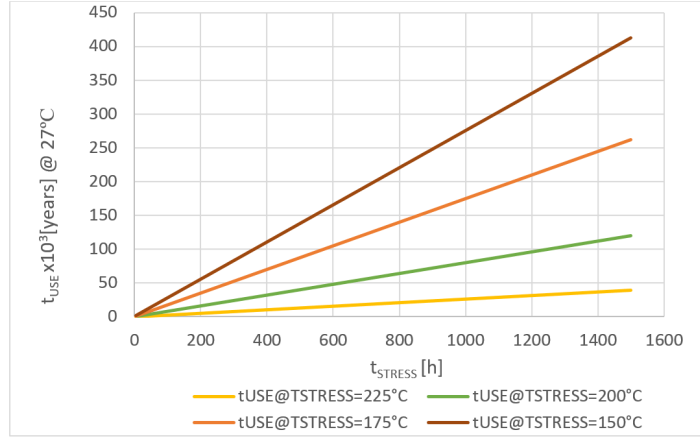


Fig. 3.: The use time t_{USE} at 27°C for stress conditions (t_{STRESS}) at diverse accelerated factors (AF).

The variation of the charge on the floating gate over time translates into a change in the FG transistor threshold voltage, V_{TH} . It is preferable that V_{TH} be used when studying retention, since it is easier to measure and it has a direct effect in circuit operation. Since the purpose of this investigation is determining the variation of the threshold voltage over time (with respect to a target threshold voltage, V_{THT}):

$$\Delta V_{TH} = V_{TH}(t_{USE}) - V_{TH}(t_0) \quad (3.6)$$

will be used to express retention experiments results. In eq. (3.6):

- $V_{TH}(t_{USE})$ is the threshold voltage of the FG transistor after being used in normal conditions for a duration equal to t_{USE} ;
- $V_{TH}(t_0)$ is the programmed threshold voltage value (the value which will be obtained after the programming process - initially targeted value is V_{THT}).

If (3.1) is taken into consideration, the threshold voltage variation can be expressed as:

$$\Delta V_{TH} = V_{TH}(AF \cdot t_{STRESS}) - V_{TH}(t_0) \quad (3.7)$$

Relation (3.7) suggests that the variation of the threshold voltage under normal use can be determined based on its variation under stress conditions.

4. The proposed reset controller circuit

A. System Description

Reset controllers are employed in many applications to monitor the voltage of a power supply. A voltage supervisor topology, proposed in this paper, is shown in Fig. 4. The schematic includes a hysteresis comparator (Comp) and a delay logic block. The comparator utilizes a reference

voltage V_{REF} (variable with respect to V_{DD}), which is accurately programmed during test mode [13–16]. The programmed value of the voltage reference depends on the monitored V_{DD} supply. The delay logic block comprises a timeout generator, which uses a counter. The clock signal is provided by an oscillator. The output of the circuit is driven by a push-pull stage, formed with transistors M_1 and M_2 .

In Fig. 4, capacitors C_1 and C_2 are used as a capacitive divider, necessary in order to obtain a fraction of V_{DD} . The resulting voltage is applied on the non-inverting input of the comparator and is given by:

$$V_{DIV} = \frac{C_1}{C_1 + C_2} \cdot V_{DD} \quad (4.1)$$

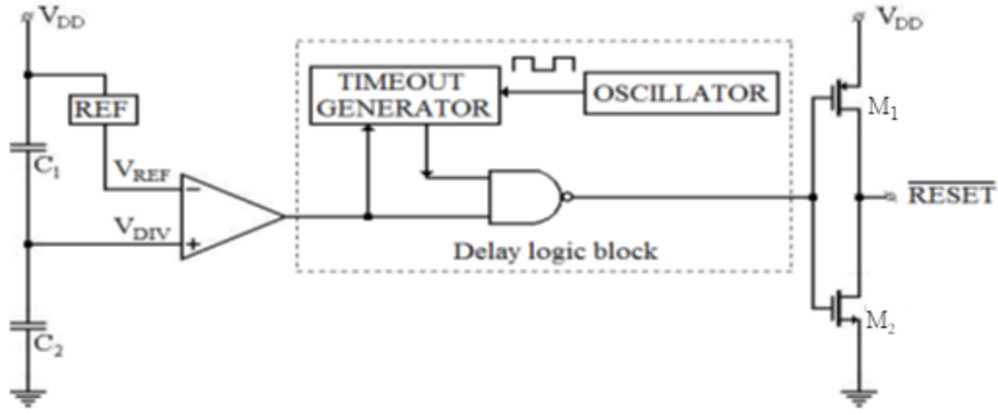


Fig. 4.: Reset controller block schematic.

The implementation of the voltage divider for obtaining V_{DIV} with capacitors leads to reduced area and current consumption, compared to other solutions [15]. The power supply threshold voltage (V_{TP}) is the minimum power supply voltage for which $\overline{RESET} = 1$. When V_{DD} is equal to the threshold voltage, $V_{REF} = V_{DIV}$. Thus, based on relation (4.1), the V_{TP} expression is obtained:

$$V_{TP} = \frac{C_1 + C_2}{C_1} \cdot V_{REF}(V_{DD}) \Big|_{V_{DD}=V_{TH}} \quad (4.2)$$

As seen in (4.2), this topology allows for the circuit to have a power supply threshold voltage higher than the reference voltage. The reset controller monitors the voltage of the power supply V_{DD} and, using the comparator, determines if it falls below a programmed V_{TP} value. As soon as this happens, the comparator output becomes logic “0” and the signal is asserted low. When V_{DD} rises above the threshold value, the comparator output switches to logic “1” and the timeout generator is triggered. After a certain delay time (T_R), fixed by the Timeout Generator, the \overline{RESET} output is set high by the logic blocks.

B. Implementation of the comparator

One of the essential blocks used in the reset controller is the comparator [15]. The proper operation of this comparator is conditioned by the accuracy of the voltage reference [14]. The latter provides a stable voltage that is precisely programmed at the wafer level.

A recent approach in integrated circuits consists of using voltage references based on flash devices [6]. One advanced method for designing this type of voltage reference includes a storage transistor with a floating gate (FG).

The schematic of the comparator is shown in Fig. 5. This simple topology was chosen because it fulfills the requirements of the current application in a satisfactory manner. For the reset controller, propagation time and offset are important, while gain and resolution are not essential (power supply voltage drops are usually large enough to be easily detectable).

In Fig. 5, the differential pair transistors Q_1 and Q_2 are FG devices. The TD FG transistor with an open source, behaves as a tunnel diode. Thus, TD is used during the programming process, which involves the pins CG (the gate of the FG Q_1 cell) and PD (the programmable drain of the FG Q_1 cell).

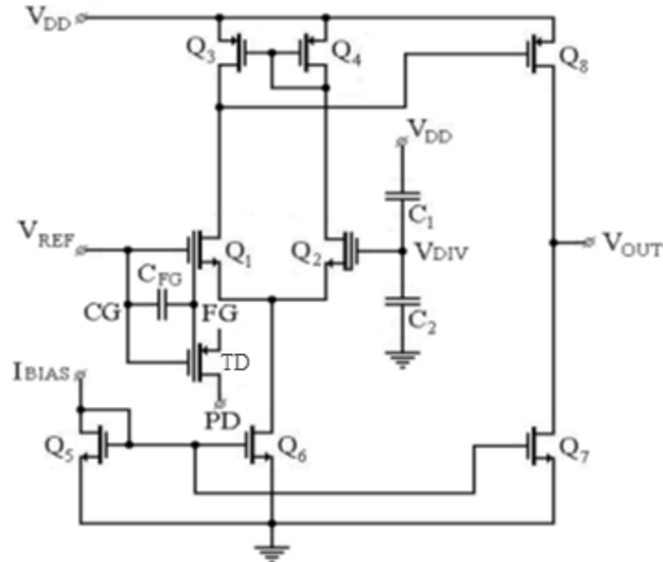


Fig. 5.: Comparator Schematic.

The voltage reference is defined by the charge stored on the floating gate of the storage transistor Q_1 . As such, by appropriate programming [16], the reference can be assigned any voltage value (the programmed value depends on the monitored V_{DD} voltage). During test mode, a negative voltage (V_{SS}) is applied on the CG and PD of the FG cell. In this manner, the threshold voltage of Q_1 is set to a determined value, ensuring a predictable behavior for the FG transistors. The applied negative voltage is imposed by the desired value of V_{REF} . The systematic offset is cancelled by the FG programming, which, together with an accurately programmed V_{REF} , leads to a well-defined power supply threshold value. The hysteresis of the comparator is obtained in an efficient manner (no quiescent current consumption), using the feedback topology described in [15].

The comparator biasing is done by the current mirror formed with transistors Q_5 , Q_6 and Q_7 . The current I_{BIAS} is generated by an internal Widlar current source. In Fig. 6, the input and output waveforms for the comparator are shown. The voltage reference is referenced to the power supply (initially V_{REF} is equal to V_{FG}). The voltage on the non-inverting input V_{DIV} is a fraction of the V_{DD} voltage.

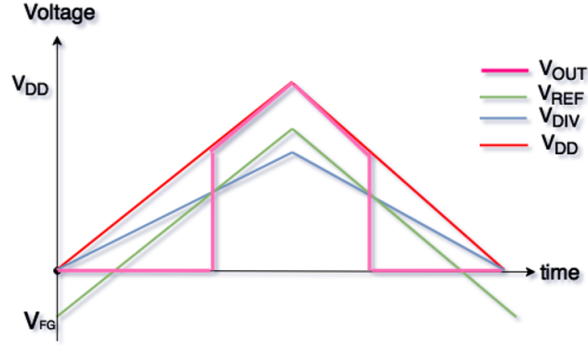


Fig. 6.: Comparator input/output theoretical waveforms.

As V_{DD} rises, the voltages on the two inputs of the comparator also increase. Initially, for low power supply voltages, $V_{DIV} > V_{REF}$ and the output of the comparator is low. Since V_{DIV} is only a fraction of the supply voltage, it increases more slowly than V_{REF} . When V_{DD} reaches the threshold value (at which V_{REF} exceeds the non-inverting inputs voltage, V_{DIV}), the comparator output switches to logic “1”.

5. Experimental Results

A. Reset controller simulations and measurements

The process used for modeling the devices was Deep N-well 0.35 μ m CMOS 5V. The circuit was simulated with the HSPICE simulator tool. The layout of the reset controller was done in Tanner L-Edit. Two versions of the proposed reset controller were implemented.

Table 1 shows the simulated results for the following circuit parameters: T_D – the delay time of the comparator and T_R – the reset active timeout period (additional delay for leaving the RESET state). These parameters were analyzed at temperatures -40°C, 25°C and 125°C and in all process corners via transient simulations, for an initial version of the reset controller. A fairly high comparator response time can be observed. The timeout reset active period is in the 220–300 ms range.

The same parameters were also measured on 13 packaged circuit samples of the first implementation, at the same temperatures. The experimental results, averaged across all investigated circuits, are given in Table 2.

A good agreement is observed between simulation and experimental results. The minor differences between values can be attributed to the limitations of the simulation models and the relatively low number of measured samples.

Table 1.: Simulated values for reset controller parameters

Parameter	Value		
	Min	Typ	Max
T_D @ 3.3V & 5.5V	5.1 μ s	10.0 μ s	20.1 μ s
T_R @ 3.3V	180 ms	232 ms	280 ms
T_R @ 5.5V	220 ms	260 ms	300 ms

Table 2.: Circuit parameters measured across 13 samples

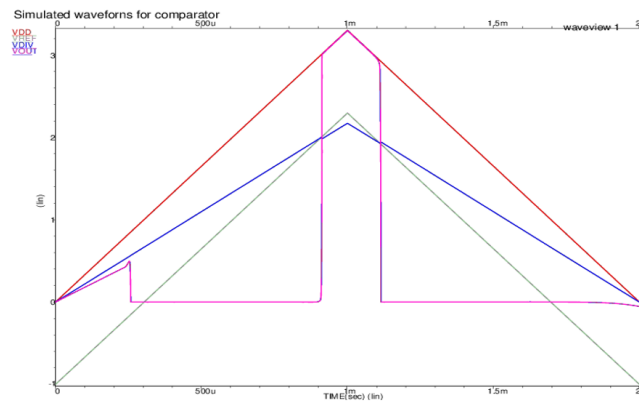
Parameter	Value		
	Min	Typ	Max
T_D @ 3.3V & 5.5V	6.1 μ s	11.4 μ s	22.1 μ s
T_R @ 3.3V	175 ms	230 ms	294 ms
T_R @ 5.5V	192 ms	245 ms	313 ms

Improvements were made in the second implementation of the circuit, especially with regards to the comparator propagation time, by changing the aspect ratio of the transistors in the output stage of the comparator. It is desirable that T_D be as low as possible, because this allows for the detection of short-lived power supply fluctuations (which can still alter the logic state of a digital circuit). The simulated values in Table 3 were obtained for the redesigned circuit. A halving of the comparator delay time can be observed.

Table 3.: Simulated values for reset controller parameters - improved circuit

Parameter	Value		
	Min	Typ	Max
T_D @ 3.3V & 5.5V	3.5 μ s	4.8 μ s	15.5 μ s
T_R @ 3.3V	195 ms	225 ms	266 ms
T_R @ 5.5V	219 ms	252 ms	299 ms

The improved comparator's operation is demonstrated by the simulated waveforms from Fig. 7 ($V_{DD} = 5.5$ V), which are in a good agreement with the theoretical plots from Fig. 6.

**Fig. 7.:** Simulated comparator input/output waveforms.

The layout of the second reset controller implementation is shown in Fig. 8. The circuit has four pads: V_{DD} , V_{SS} , GND and \overline{RESET} . The V_{SS} pad is used only at the wafer level and thus not accessible to the user. The chip dimensions are $410\mu\text{m} \times 510\mu\text{m}$.

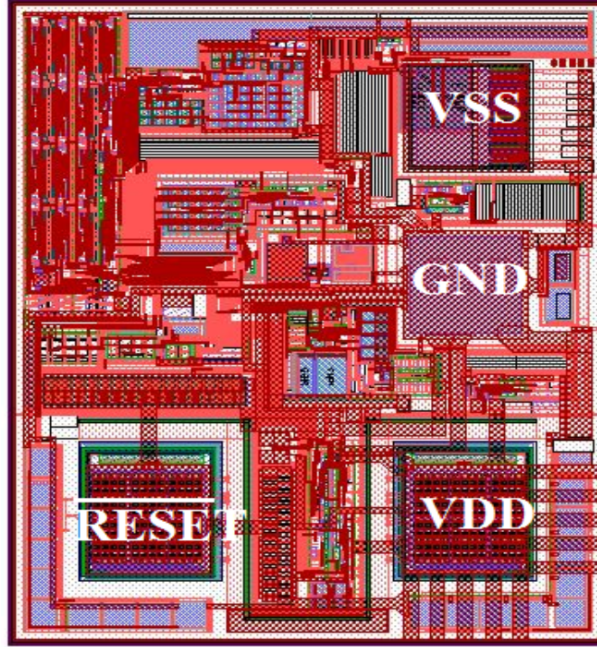


Fig. 8.: The layout of the proposed reset controller (color online).

B. Floating gate charge retention experiments

The newest experiment for this paper was focused on the charge retention characteristics of the floating gate transistors used, which constitute an essential component of the reset controller presented in this paper.

The first step of the the charge retention experiment is programming all the FG cells on a wafer at 27°C . After this process, approximately 1.2% FG cells failed, losing their charge. The remaining devices were subjected to a stress temperature of 225°C , performed in an oven with nitrogen ambient. The stress times used ranged from 24h to 1500h. Naturally, in order to evaluate retention, the threshold voltage (dependent on the FG charge) of the devices was measured.

In the manner described above, the dependence of the relative variation of the threshold voltage on a wafer (initially targeted for V_{THT} equal to 2.5V, 3.5V and respectively 4.5V) on stress time is obtained (Fig. 9). For the plots in Fig. 9, the average threshold voltage evaluated at the wafer level was considered (based on this value the relative variation was determined).

As the stress time is raised, the stored charge (and thus V_{TH}) also increases. For larger threshold voltages, the relative variation of V_{TH} is less than the variation for smaller thresholds, it increases significantly. For instance, after 1500h of thermal treatment, the relative average of V_{TH} , in the case of a 2.5V target threshold voltage, is 217ppm, while the same scenario for $V_{THT} = 4.5\text{ V}$ gives a variation of 86 ppm.

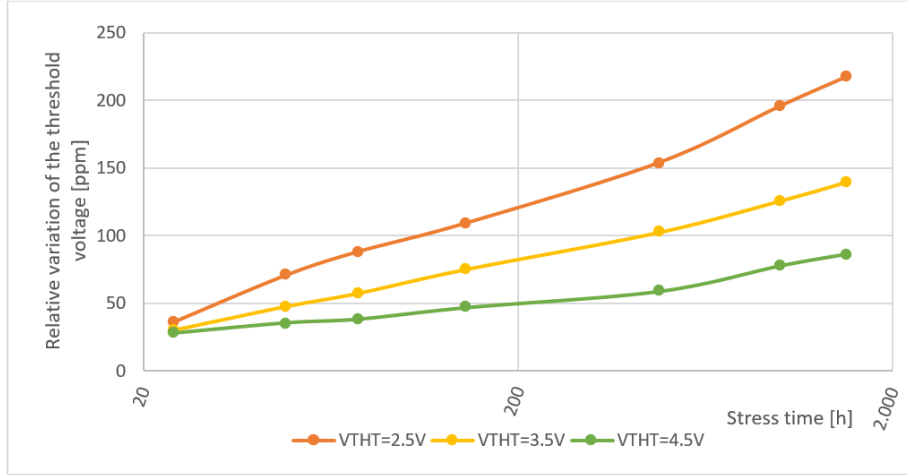


Fig. 9.: Relative variation of the threshold voltage vs. stress time (color online).

The variation of the relative average of the threshold voltage is further interpreted in Table 4. The programmed FG cells are functional under stress for 1500h at 225°C. This means that at 2°C, the relative threshold voltage will vary by an average of approximately 147ppm in 39945 years, as can be seen in Table 5. The values presented in Table 5 were determined using the analytical method described in Section 3 (similar to the plots in Fig. 3).

Table 4.: The relative variation of the threshold voltage with stress time at a stress temperature of 225°C

$t_{STRESS}[h]$	24	48	75	145	477	1000	1500
$\Delta V_{TH}[ppm]@V_{THT} = 2.5V$	35.8	70.6	88.1	109.1	153.9	195.3	217.1
$\Delta V_{TH}[ppm]@V_{THT} = 3.5V$	29.9	47.5	57.3	74.9	102.4	125.6	139.4
$\Delta V_{TH}[ppm]@V_{THT} = 4.5V$	27.9	35.5	38.2	46.6	58.6	77.5	86.1

Table 5.: Thermal treatment acceleration effect (225°C stress vs. 27°C normal used)

$t_{STRESS}@225^{\circ}C$	24h	48h	75h	145h	477h	1000h	1500h
$t_{SE}@27^{\circ}C$	630	1260	2000	3806	12671	26821	39945
	years	years	years	years	years	years	years

The evolution of the wafer-level yield (*i.e.* the percentage of FG cells operating properly) with stress time for the three desired threshold voltages is presented in Fig. 10. After programming the FG cells, the yield decreased by approximately 3%. The constancy of the yield values beyond this initial decrease (in all three cases) demonstrates the high reliability of the process. These results and the ones presented in Fig. 9 suggest that the designed reset controller could operate properly for prolonged period of time and that, if any failure occurs, it is unlikely to have been caused by the FG cell.

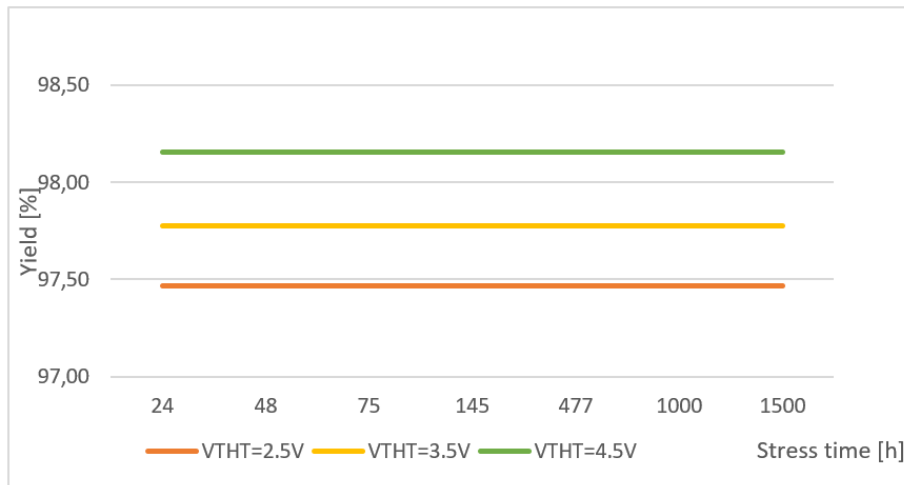


Fig. 10.: Yield evolution of the normalized average threshold voltage under the thermal treatment process (color online).

Distributions of the threshold voltage variation, as expressed in (3.6), were obtained experimentally for several wafers and two target values (2.5 V and 4.5 V). The evolution of these distributions under thermal treatment (after 24h, 100h and 1500h) was also investigated, resulting in plots in Fig. 11 – Fig. 16. All means and standard deviations are expressed in mV.

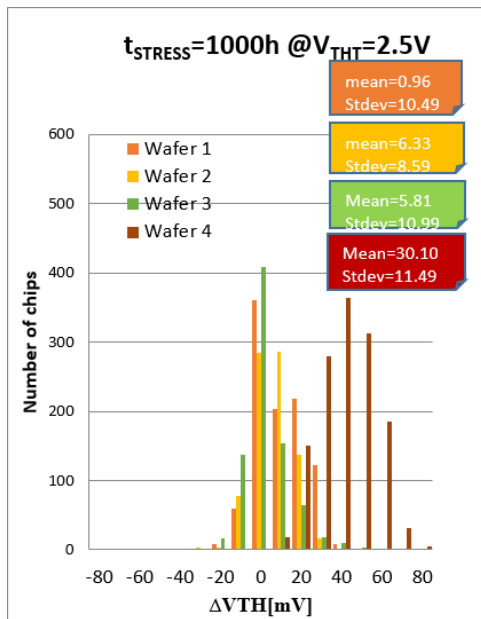


Fig. 11.: Threshold voltage distribution for 24h stress time at target value 2.5V

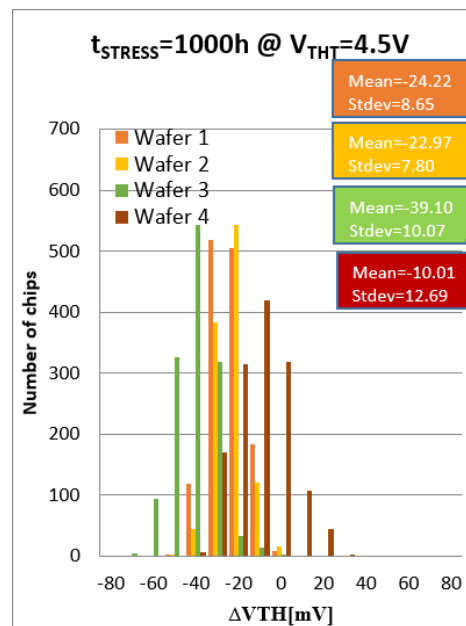


Fig. 12.: Threshold voltage distribution for 24h stress time at target value 4.5V

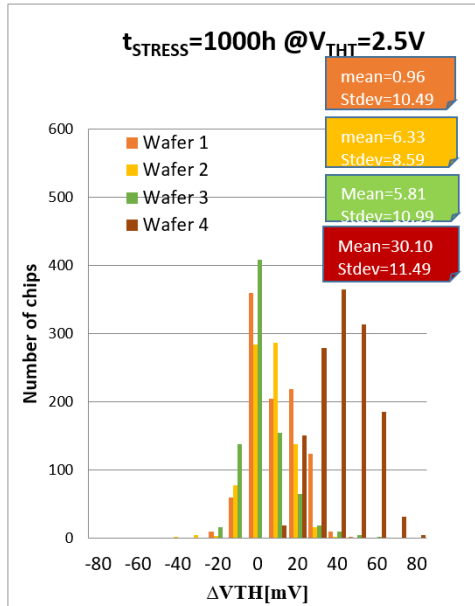


Fig. 13.: Threshold voltage distribution for 1000h stress time at target value 2.5V

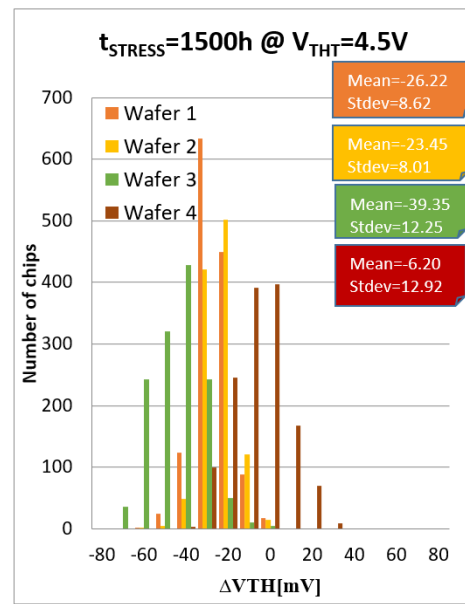


Fig. 14.: Threshold voltage distribution for 1000h stress time at target value 4.5V

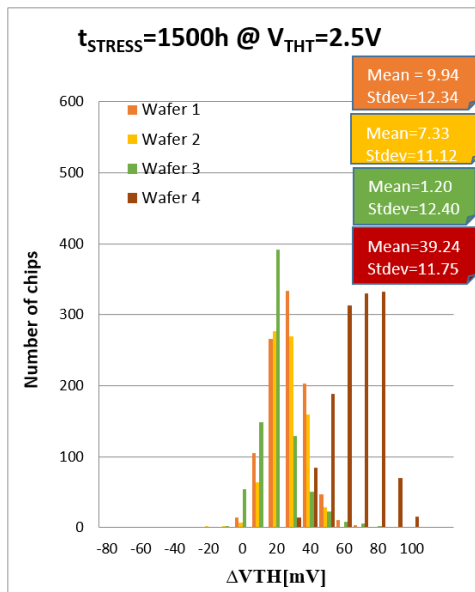


Fig. 15.: Threshold voltage distribution for 1500h stress time at target value 2.5V

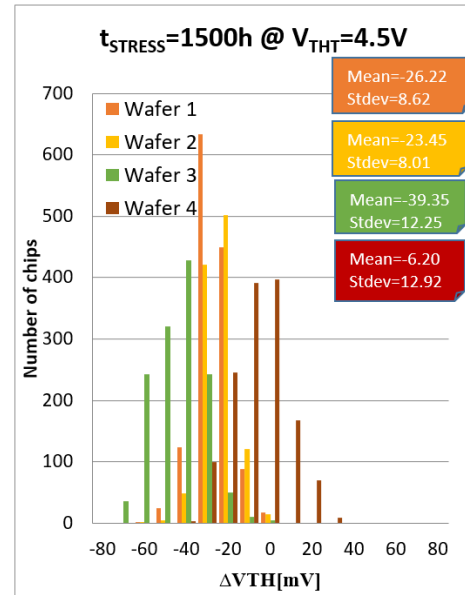


Fig. 16.: Threshold voltage distribution for 1500h stress time at target value 4.5V

Following the evolution of the distributions as stress time increased, we can observe the same behavior seen in Fig. 9 (*i.e.* the threshold voltage increases in time). After 1500h of stress times for wafer 4 with $V_{THT}=2.5V$, the variation of the threshold voltage mean is centered at 39.24mV. For the same wafer, in 99.7% of chips, the threshold voltage is between 3.99mV and 74.49mV. In the case of the 4.5V target threshold voltage (same wafer), a variation between -44.96mV and 31.56mV is observed, which means that the variation for all samples did not exceed 3% for 1500h in 39945 years.

6. Conclusions

A programmable voltage supervisor was designed, implemented and tested. The circuit generates a reset signal, when the power supply voltage is lower than a programmed threshold value. The reset controller was implemented in a Deep N-Well 5V 0.35 μ m CMOS process, which has enhanced on-chip isolation, but at a lower cost than SOI. One important advantage of this technology is that it allows for the p-substrate to be connected to the power supply voltage.

The reset controller uses a programmable voltage reference, which is built using floating gate devices. The power supply threshold voltage is dependent on the programmable voltage reference and can be set to any value demanded by the customer.

The comparator used in the voltage supervisor was redesigned to have a typical propagation time of $\sim 5 \mu s$, in order to allow for the detection of short spikes in the power supply voltage. The ~ 250 ms timeout interval is used for protecting digital circuits for an additional period of time after brownout conditions are no longer detected.

A methodology for estimating charge retention on the floating gate of a FG MOS transistor (a crucial device of the comparator used in the reset controller) was developed based on the Arrhenius model. For this purpose, a thermal treatment was applied at 225°C and the variation of the FG transistor threshold voltage was measured.

A maximum variation of around 220 ppm was observed after 1500h of thermal treatment, which is equivalent to a room temperature usage of approximately 40000 years. Note that all the FG cells resisted under the stress imposed, as evinced by the non-variant yield evolution during the thermal treatment. The distribution of the threshold voltage was determined for multiple wafers with two desired values (2.5 V and 4.5 V) and after several stress times. The maximum deviation from the target value observed for all cases was around 100 mV (after 1500h of thermal treatment).

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